FIG. 1

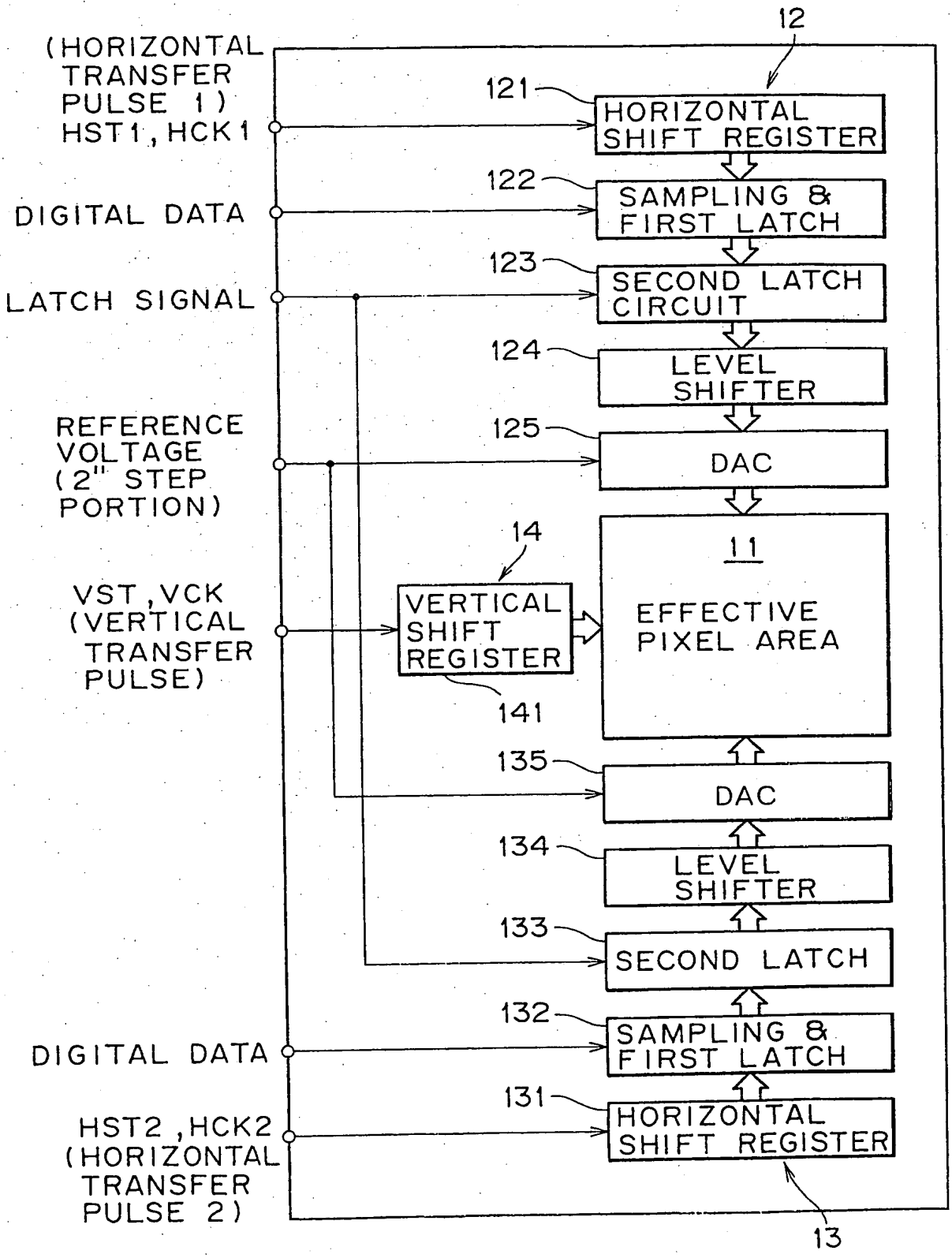

12
(HORIZONTAL TRANSFER PULSE 1) HST1, HCK1
121
HORIZONTAL SHIFT REGISTER
122
SAMPLING & FIRST LATCH
DIGITAL DATA
123
SECOND LATCH CIRCUIT
LATCH SIGNAL
124
LEVEL SHIFTER
REFERENCE VOLTAGE (2" STEP PORTION)
125
DAC
14
11
EFFECTIVE PIXEL AREA
VST, VCK (VERTICAL TRANSFER PULSE)
VERTICAL SHIFT REGISTER
141
135
DAC
134
LEVEL SHIFTER
133
SECOND LATCH
132
SAMPLING & FIRST LATCH
DIGITAL DATA
131
HORIZONTAL SHIFT REGISTER
HST2, HCK2 (HORIZONTAL TRANSFER PULSE 2)
13

FIG. 2

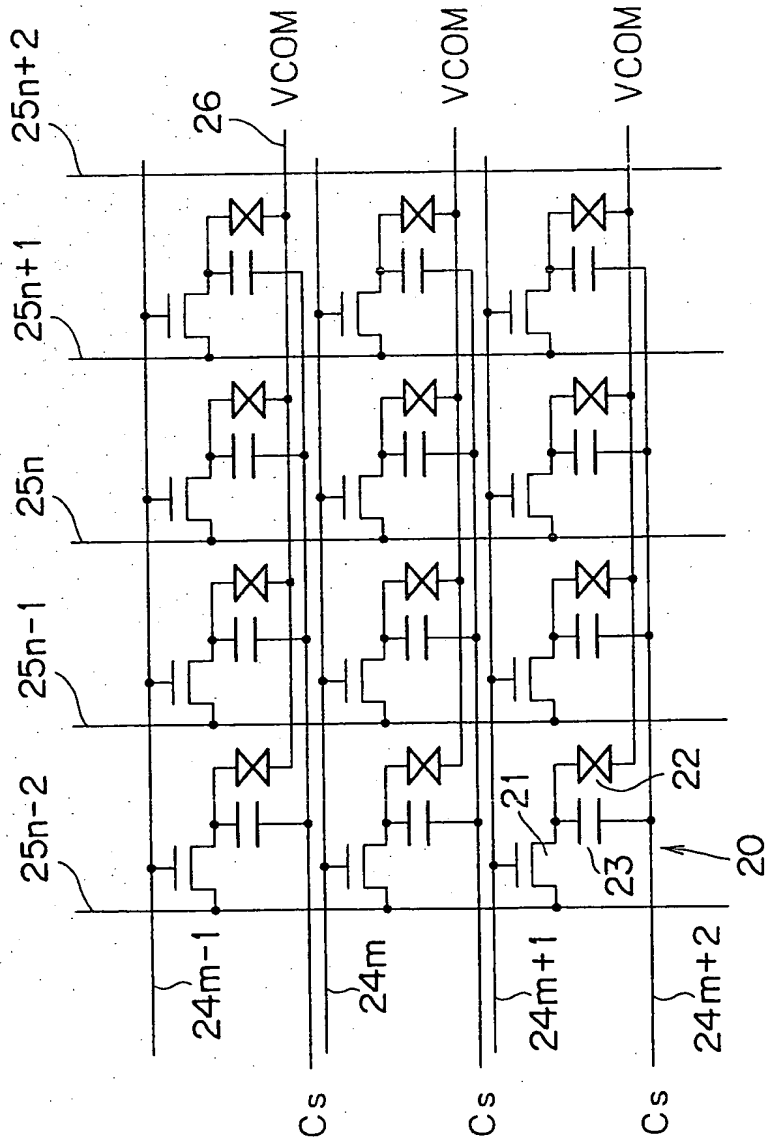

25n-2
25n-1
25n
25n+1
25n+2
26
VCOM
VCOM
VCOM
24m-1
24m
24m+1
24m+2
Cs
Cs
Cs
21
22
23
20

FIG. 3

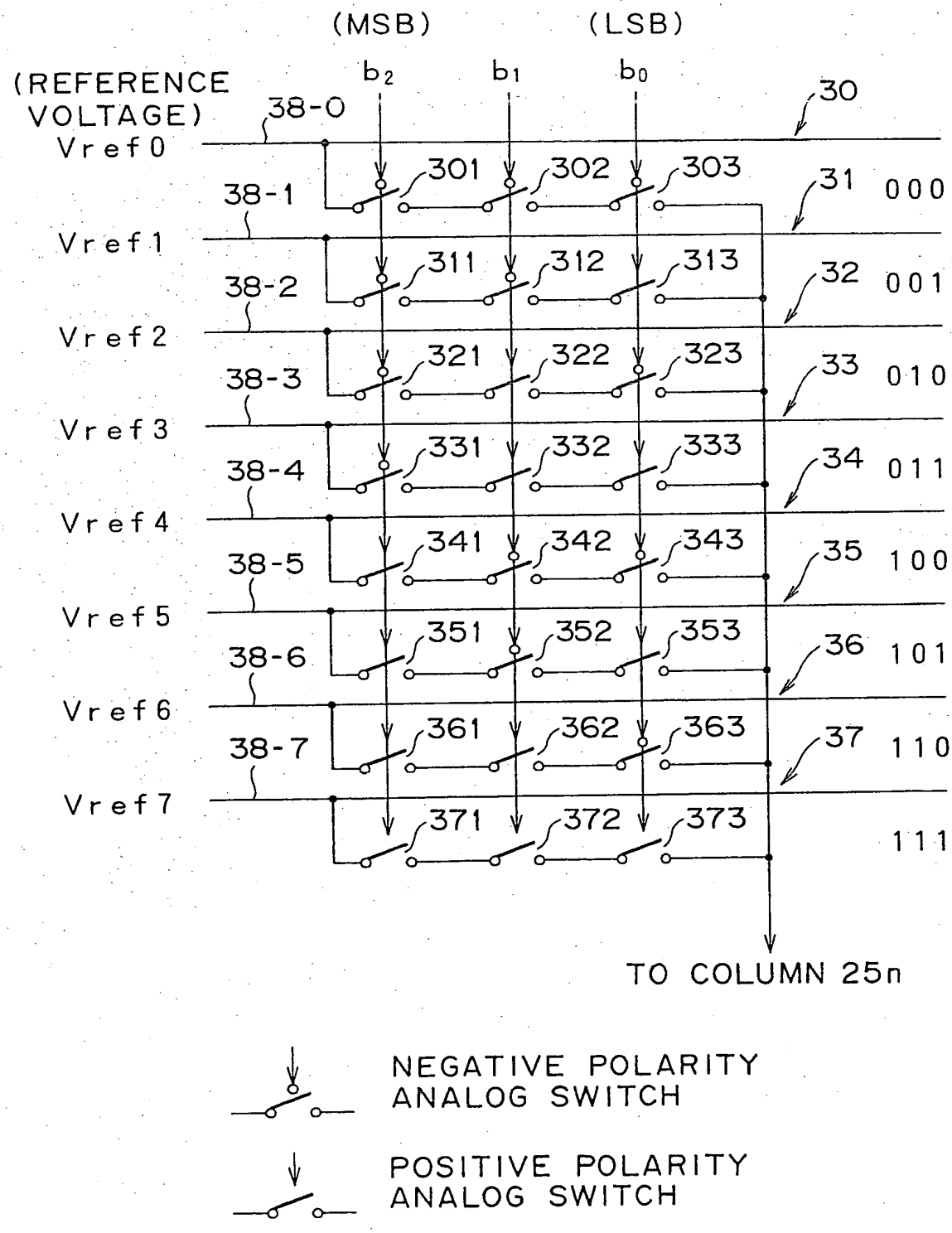

(MSB)
(LSB)
b2
b1
b0
(REFERENCE VOLTAGE)
38-0
30
Vref0
301
302
303
38-1
31
000
Vref1
311
312
313
38-2
32
001
Vref2
321
322
323
38-3
33
010
Vref3
331
332
333
38-4
34
011
Vref4
341
342
343
38-5
35
100
Vref5
351
352
353
38-6
36
101
Vref6
361
362
363
38-7
37
110
Vref7
371
372
373
111
TO COLUMN 25n
NEGATIVE POLARITY ANALOG SWITCH
POSITIVE POLARITY ANALOG SWITCH

FIG. 4

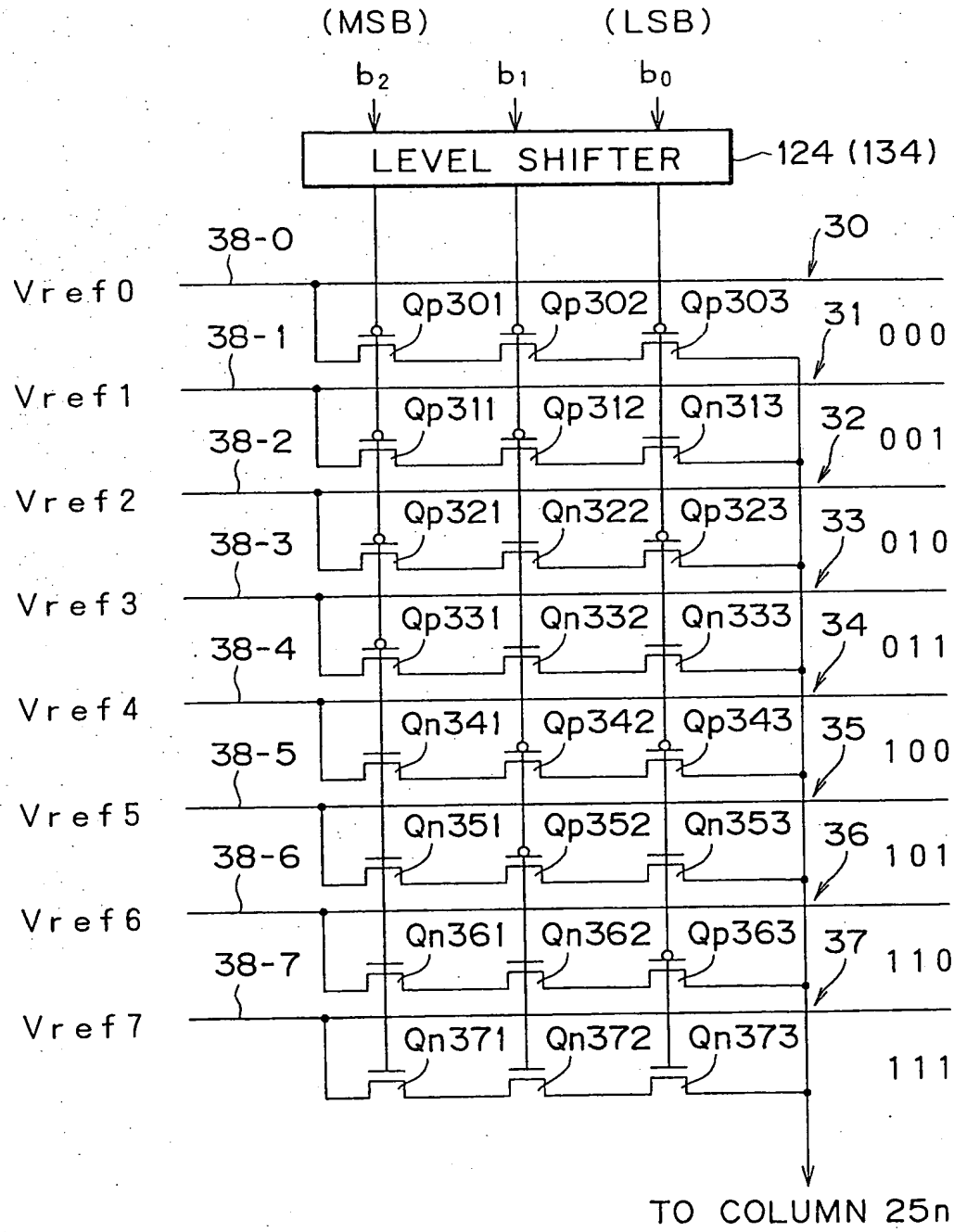

(MSB)
(LSB)
b2
b1
b0
LEVEL SHIFTER
124 (134)
30
38-0
38-1
38-2
38-3
38-4
38-5
38-6
38-7
Vref0
Vref1
Vref2
Vref3
Vref4
Vref5
Vref6
Vref7
Qp301 Qp302 Qp303
Qp311 Qp312 Qn313
Qp321 Qn322 Qp323
Qp331 Qn332 Qn333
Qn341 Qp342 Qp343
Qn351 Qp352 Qn353
Qn361 Qn362 Qp363
Qn371 Qn372 Qn373
31
32
33
34
35
36
37
000
001
010
011
100
101
110
111
TO COLUMN 25n

FIG. 5

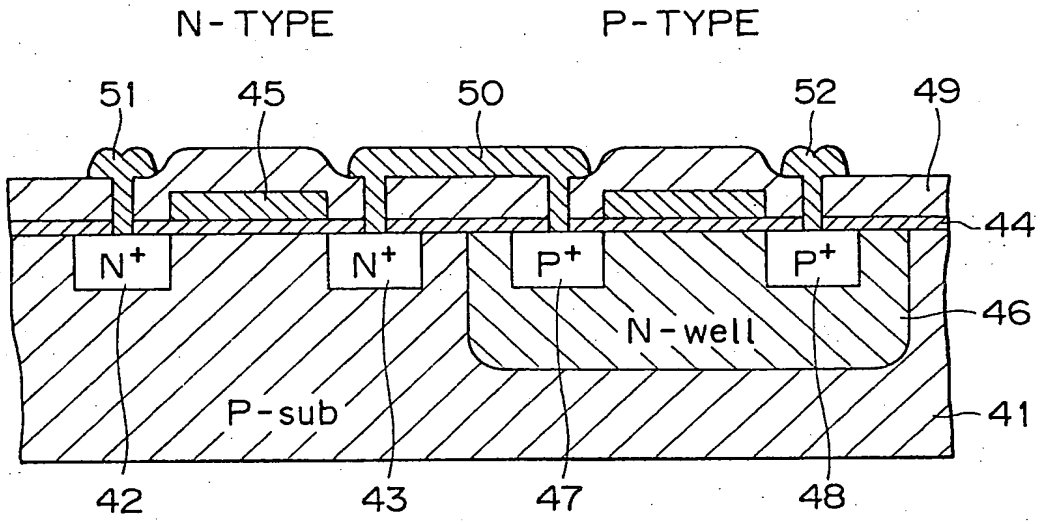

N-TYPE
P-TYPE
51
45
50
52
49
44
N+
N+
P+
P+
46
N-well
P-sub
41
42
43
47
48

FIG. 6

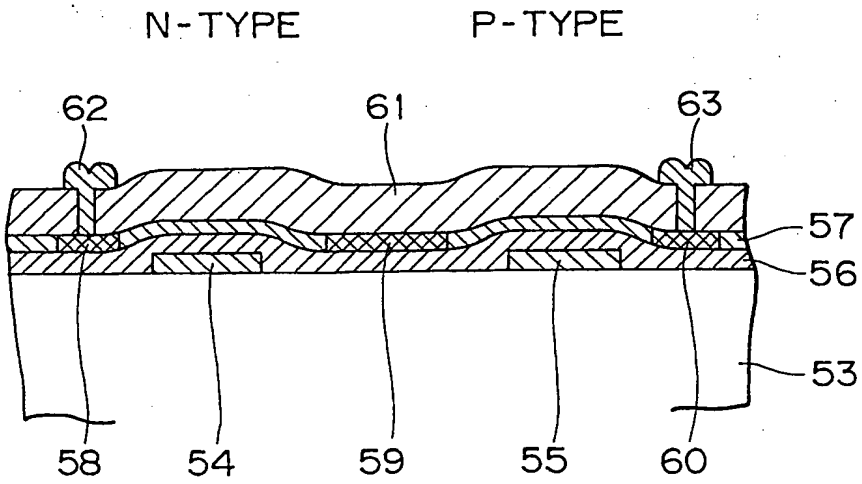

N-TYPE
P-TYPE
62
61
63
57
56
53
58
54
59
55
60

FIG. 7

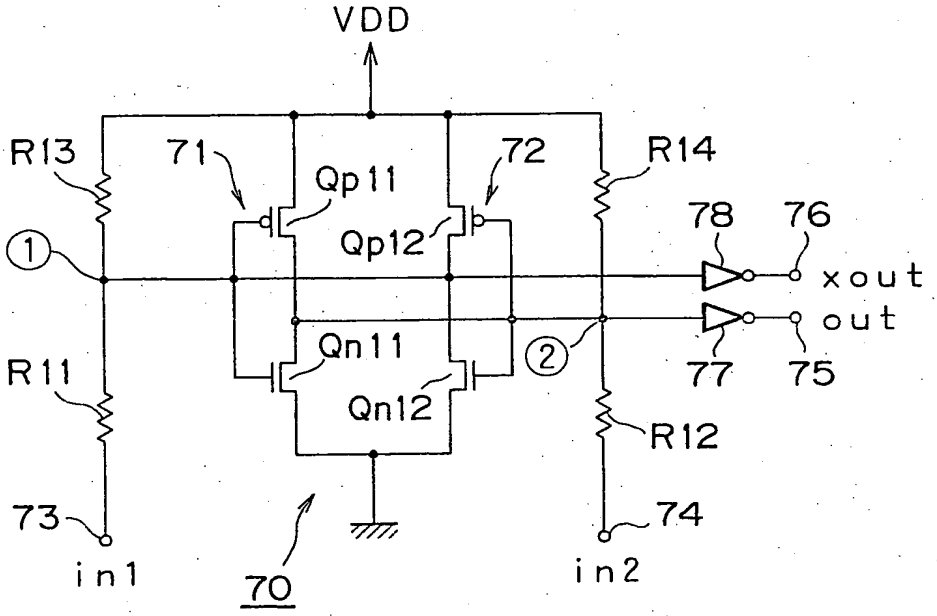

VDD
R13
71
Qp11
72
R14
78
76
①
Qp12
xout
out
Qn11
②
77
75
R11
Qn12
R12
73
74
in1
70
in2

FIG. 8

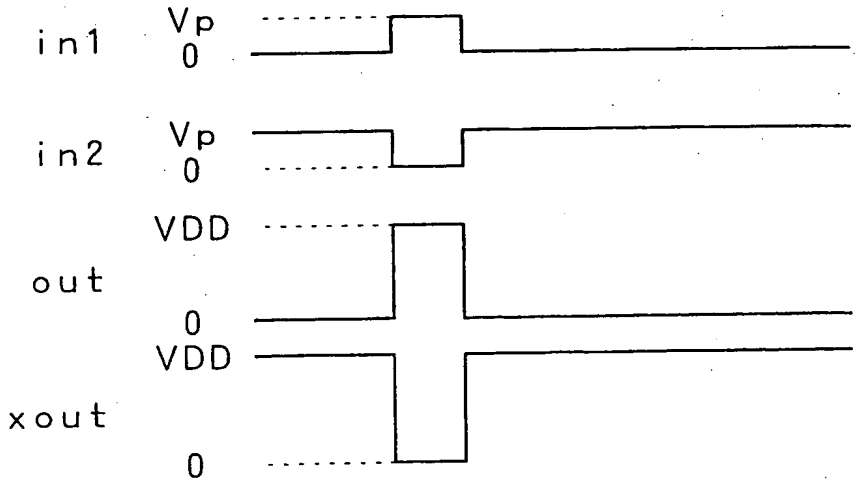

in1
Vp
0
in2
Vp
0
VDD
out
0
VDD
xout
0

FIG. 9

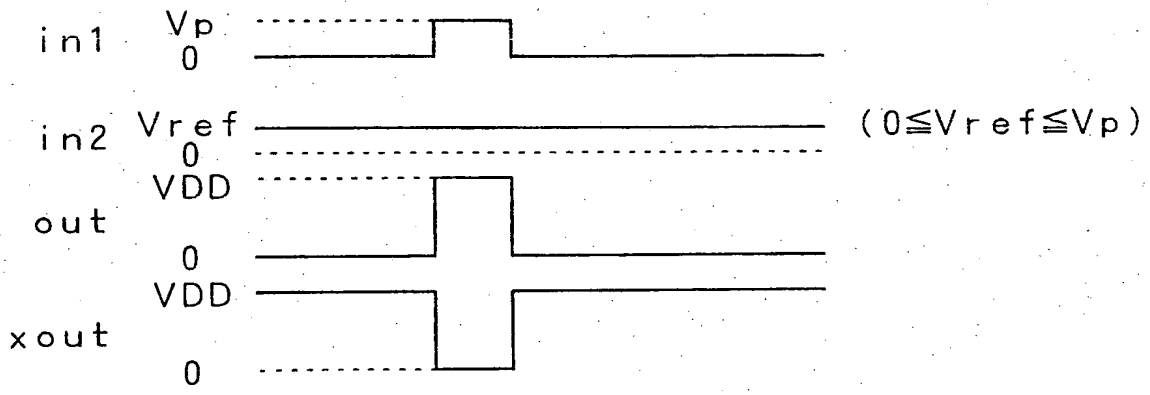

in1
Vp
0
in2
Vref
0
(0≦Vref≦Vp)
VDD
out
0
VDD
xout
0

FIG. 10

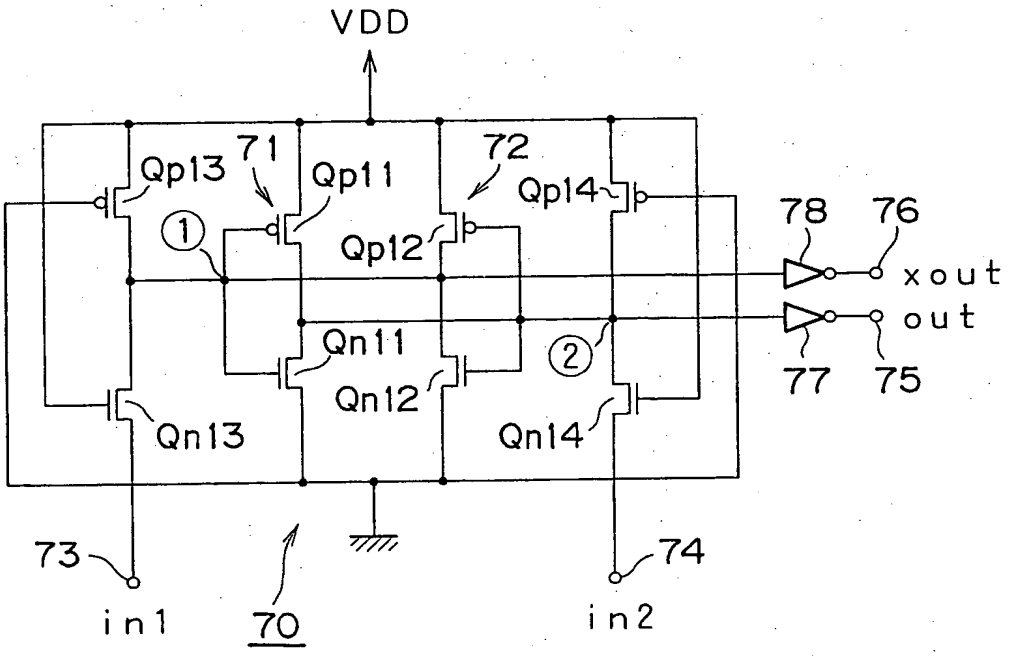

VDD
71
72
Qp13
Qp11
Qp14
①
Qp12
78
76
xout
out
Qn11
②
Qn12
77
75
Qn13
Qn14
73
74
in1
70
in2

FIG. 10B
RELATED ART

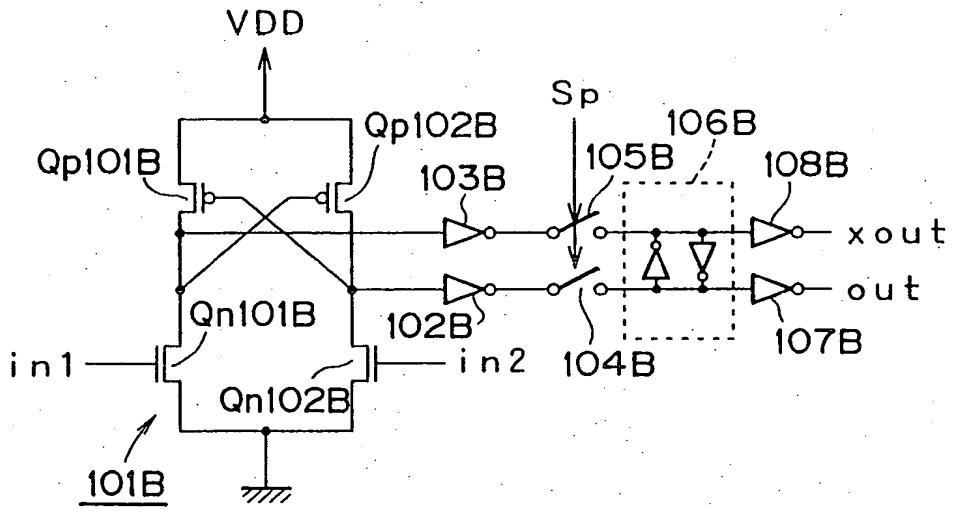


FIG. 10C
RELATED ART 1

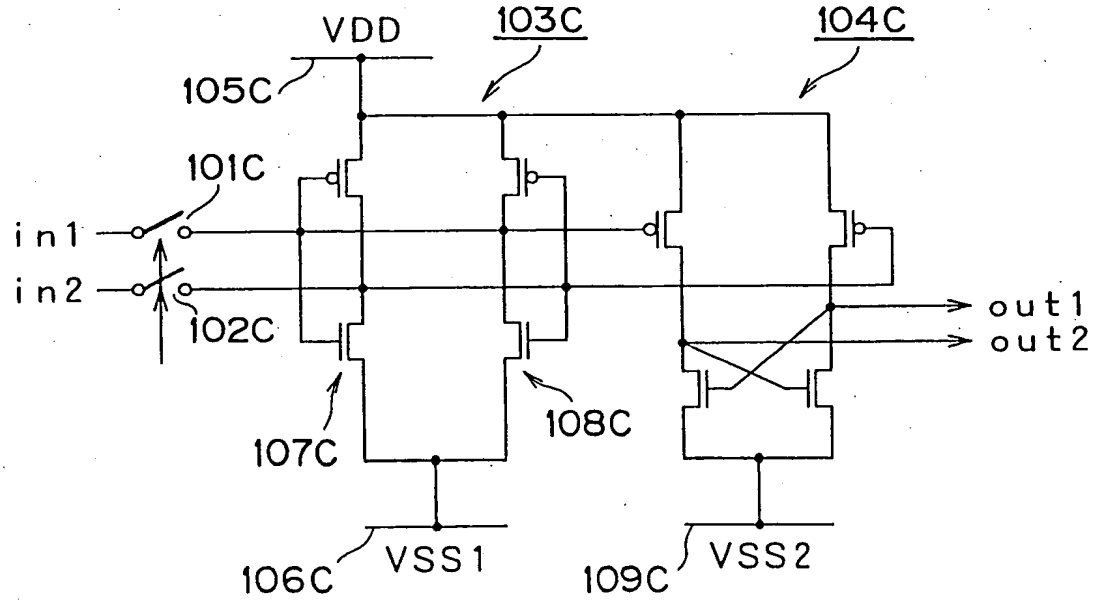


FIG. 11

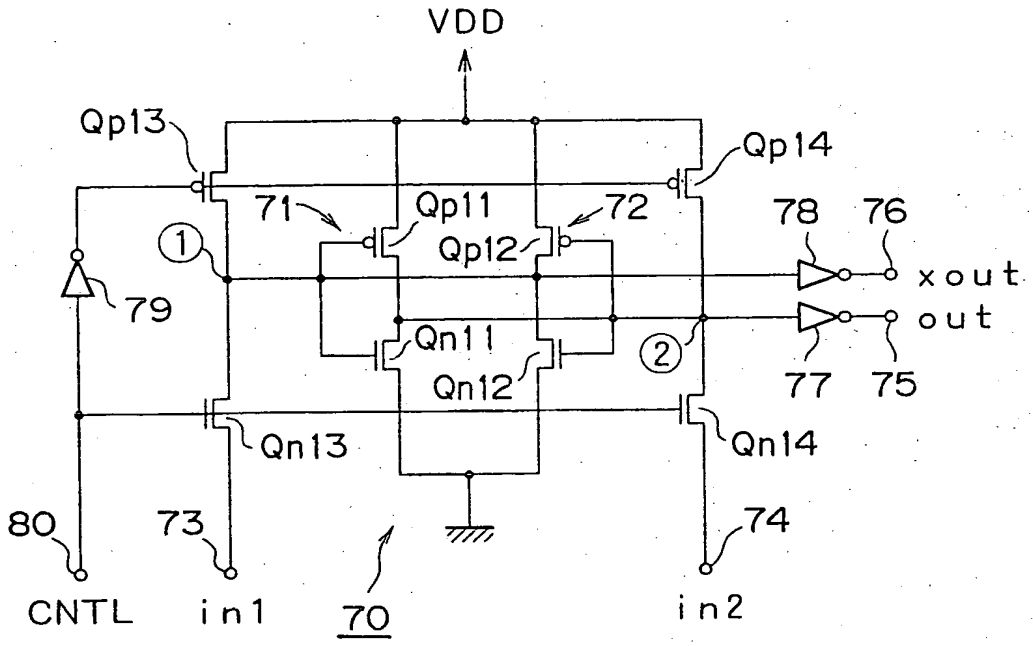


FIG. 11B
RELATED ART

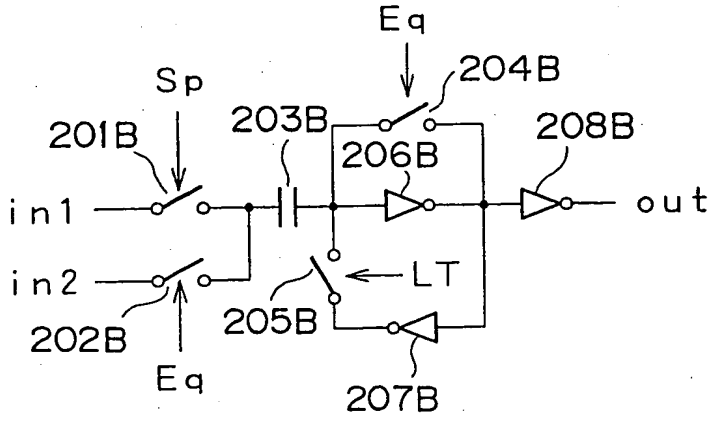


FIG. 11C
RELATED ART 2

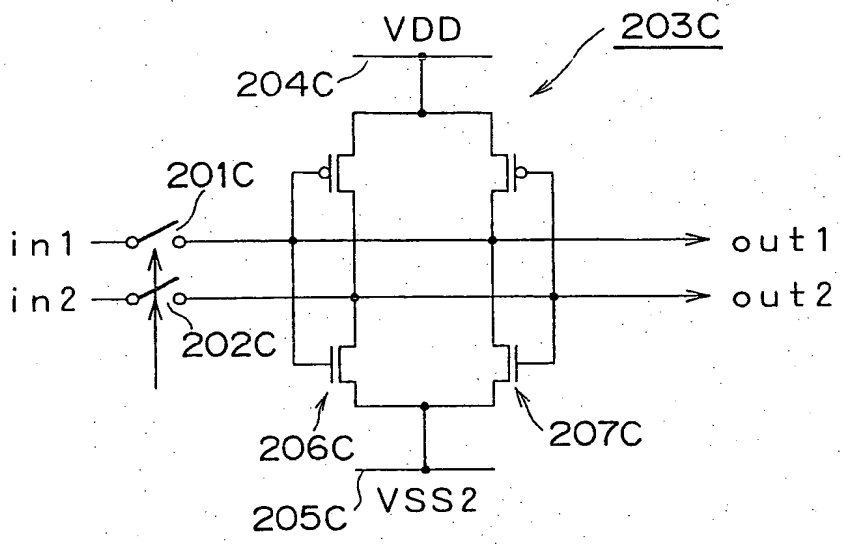


FIG. 12

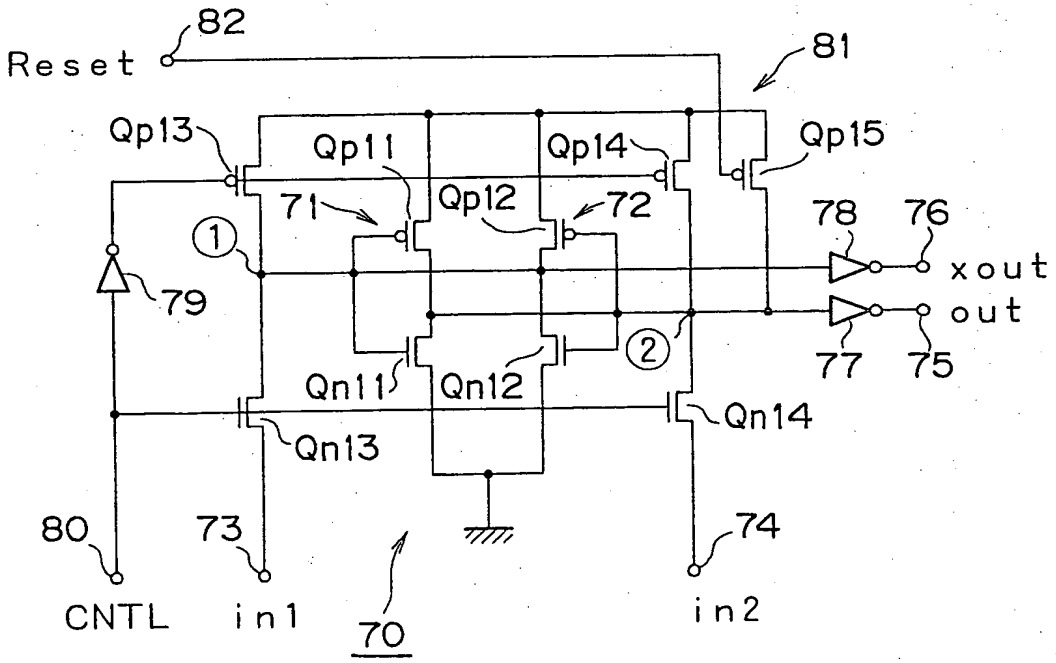


FIG. 12C
RELATED ART 3

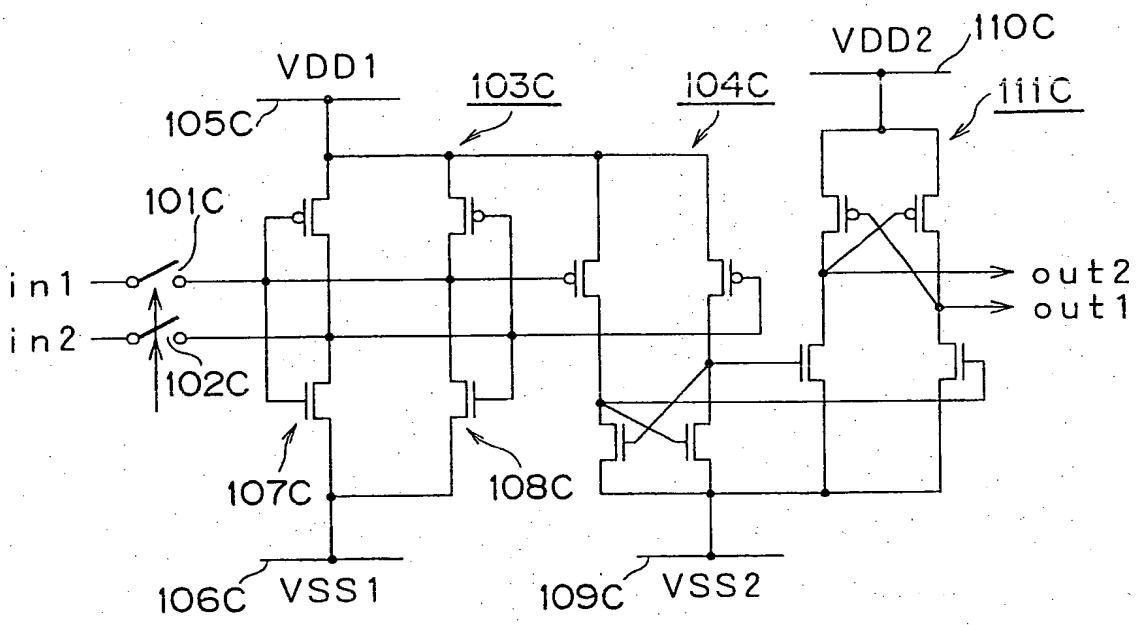


FIG. 13

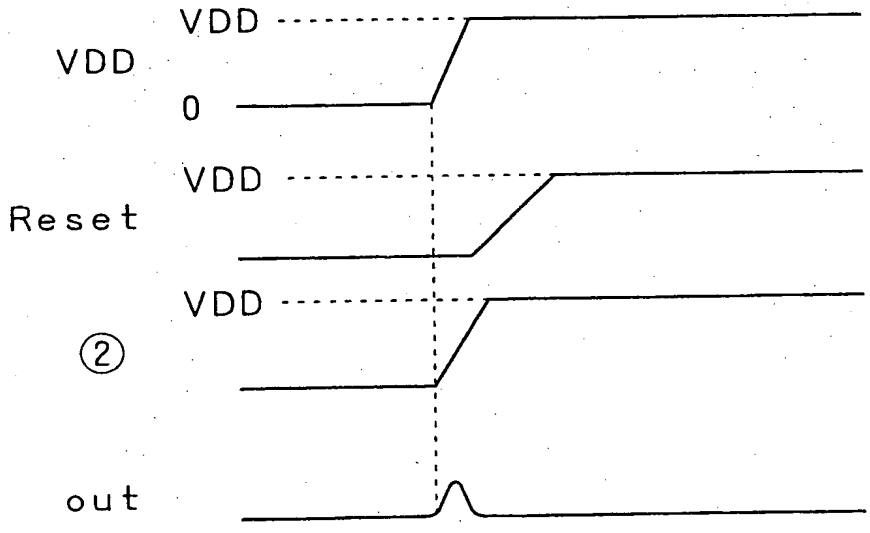


FIG. 13A
RELATED ART 1

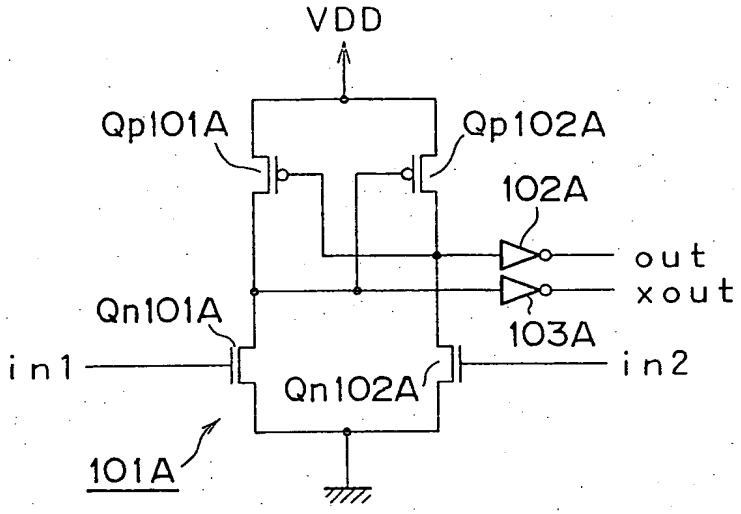


FIG. 13C
RELATED ART 4

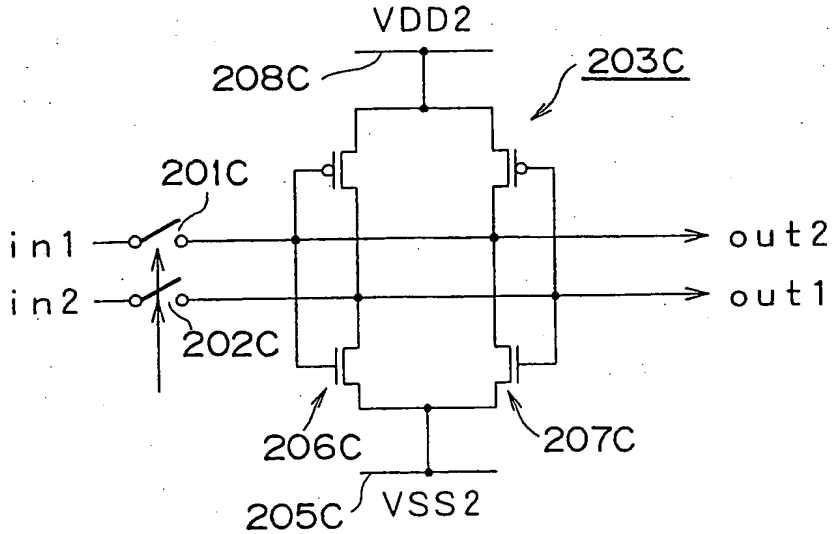


FIG. 14

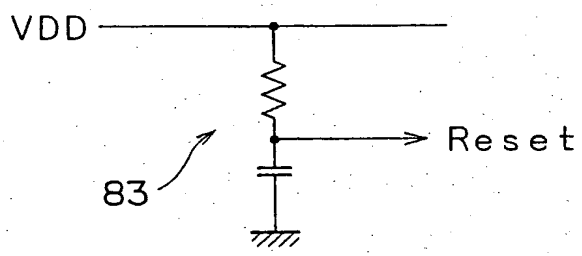


FIG. 14A
RELATED ART 2

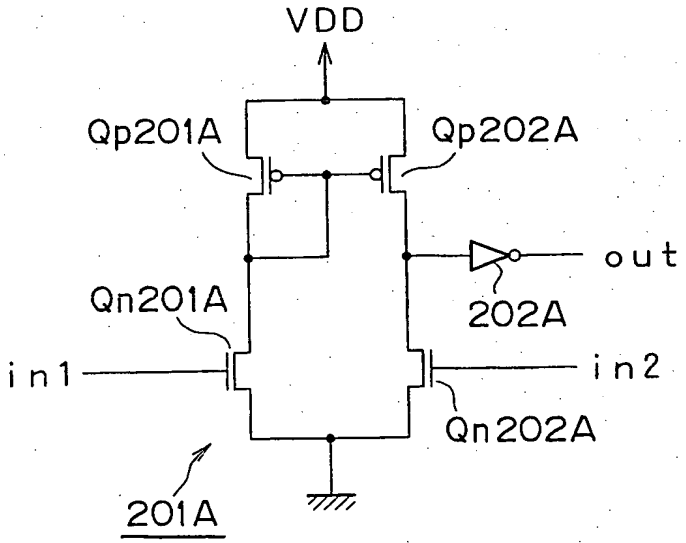


FIG. 15

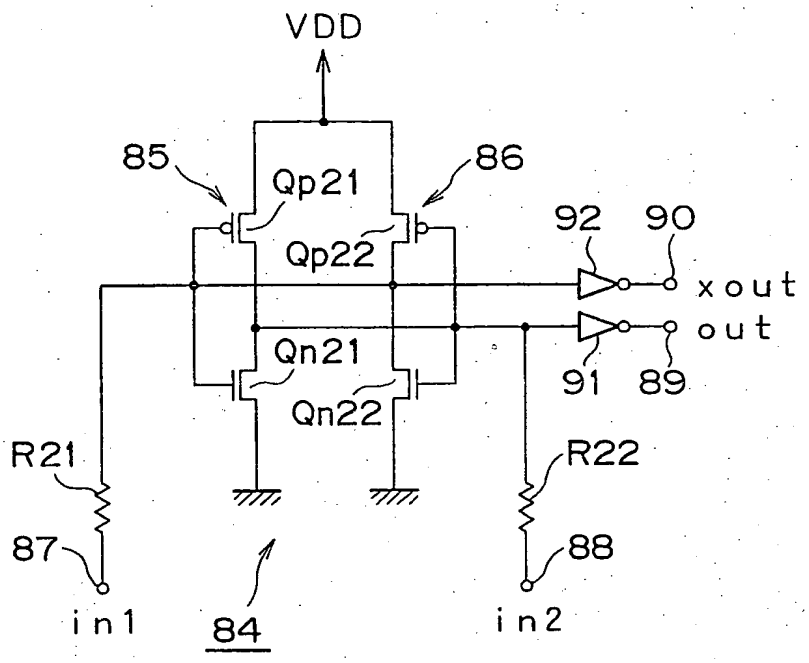


FIG. 15A
RELATED ART 3

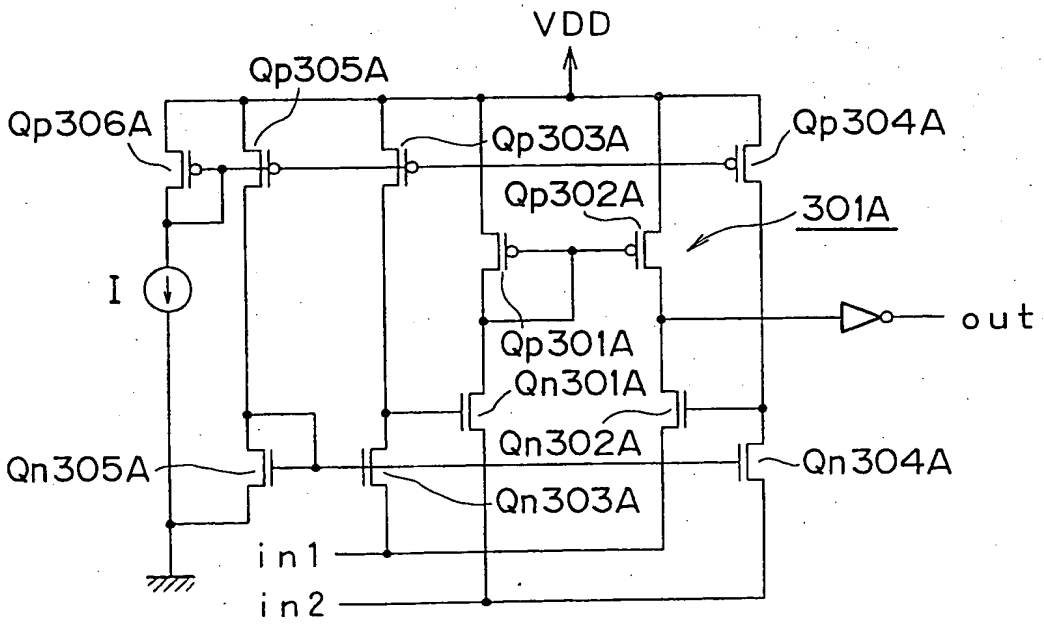


FIG. 16

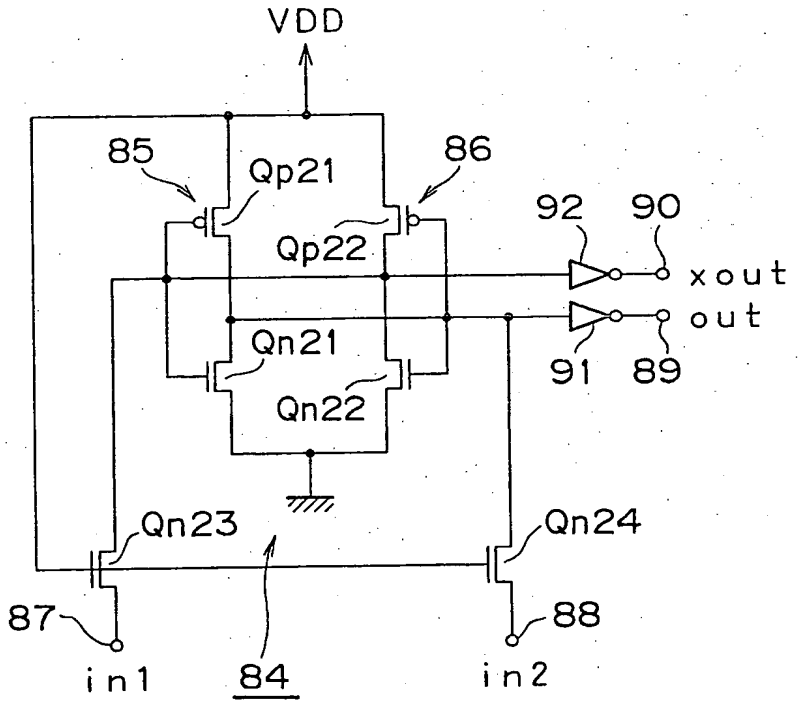

VDD
85
Qp21
86
Qp22
92
90
xout
out
Qn21
Qn22
91
89
Qn23
Qn24
87
88
in1
84
in2

FIG. 17

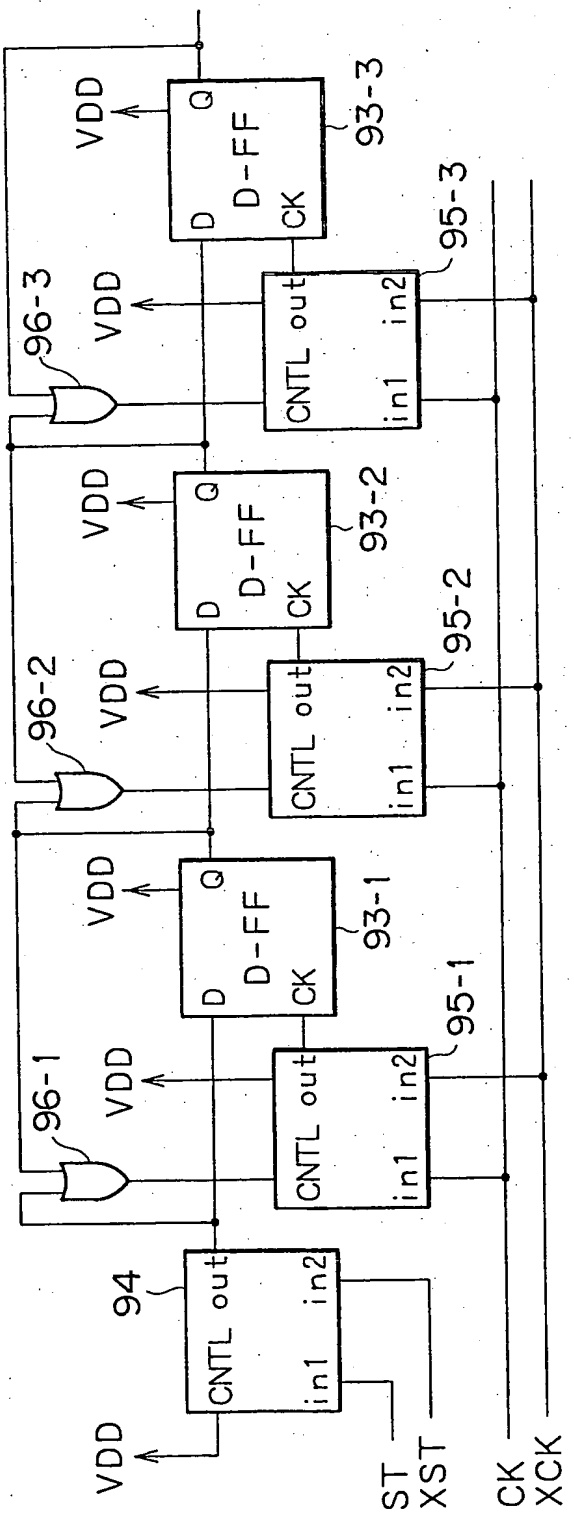

VDD
94
CNTL out
in1 in2
ST
XST
CK
XCK
96-1
95-1
93-1
96-2
95-2
93-2
96-3
95-3
93-3
D-FF
D
Q
CK

FIG. 18

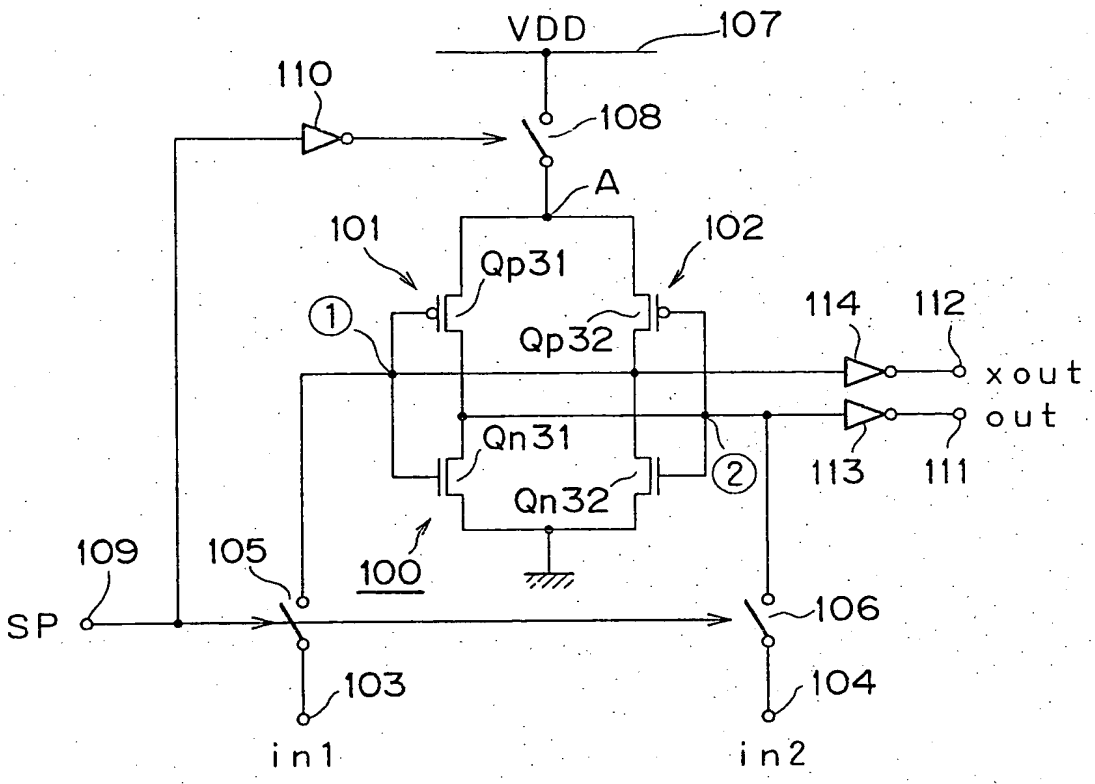

VDD
107
110
108
A
101
102
Qp31
Qp32
114
112
xout
out
Qn31
Qn32
113
111
109
105
100
106
SP
103
104
in1
in2

FIG. 19

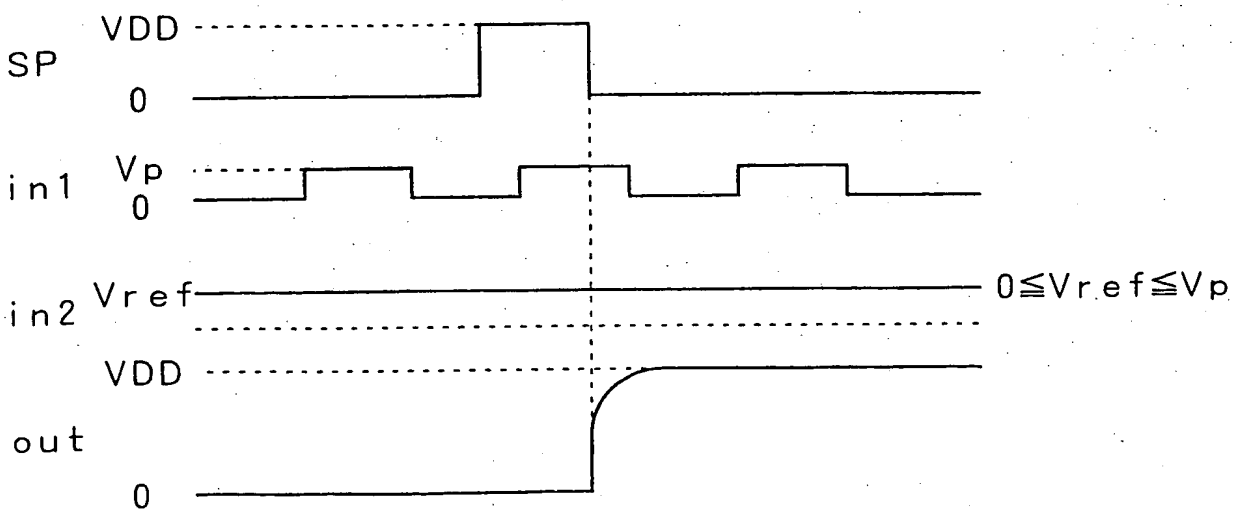

SP
VDD
0
in1
Vp
0
in2
Vref
0≦Vref≦Vp
VDD
out
0

FIG. 20

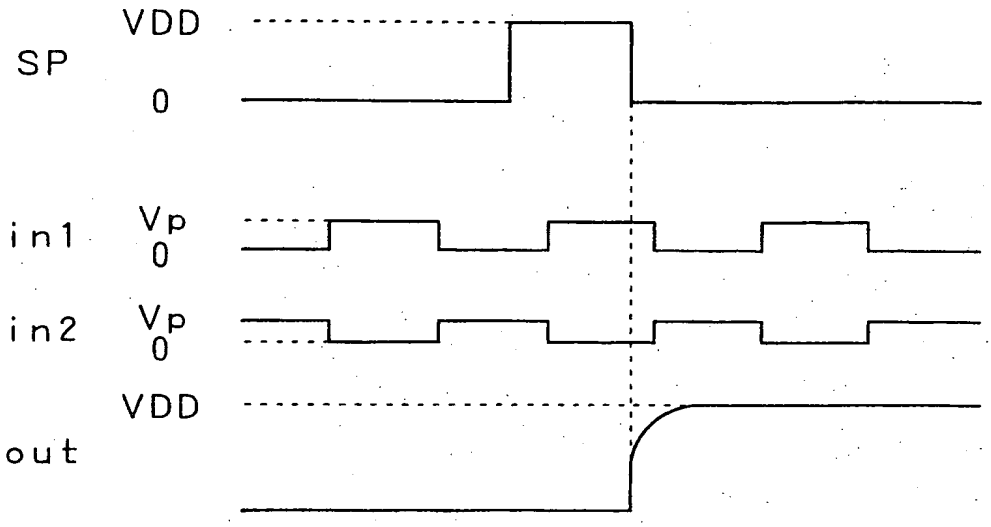

VDD
SP
0
in1
Vp
0
in2
Vp
0
VDD
out

FIG. 21

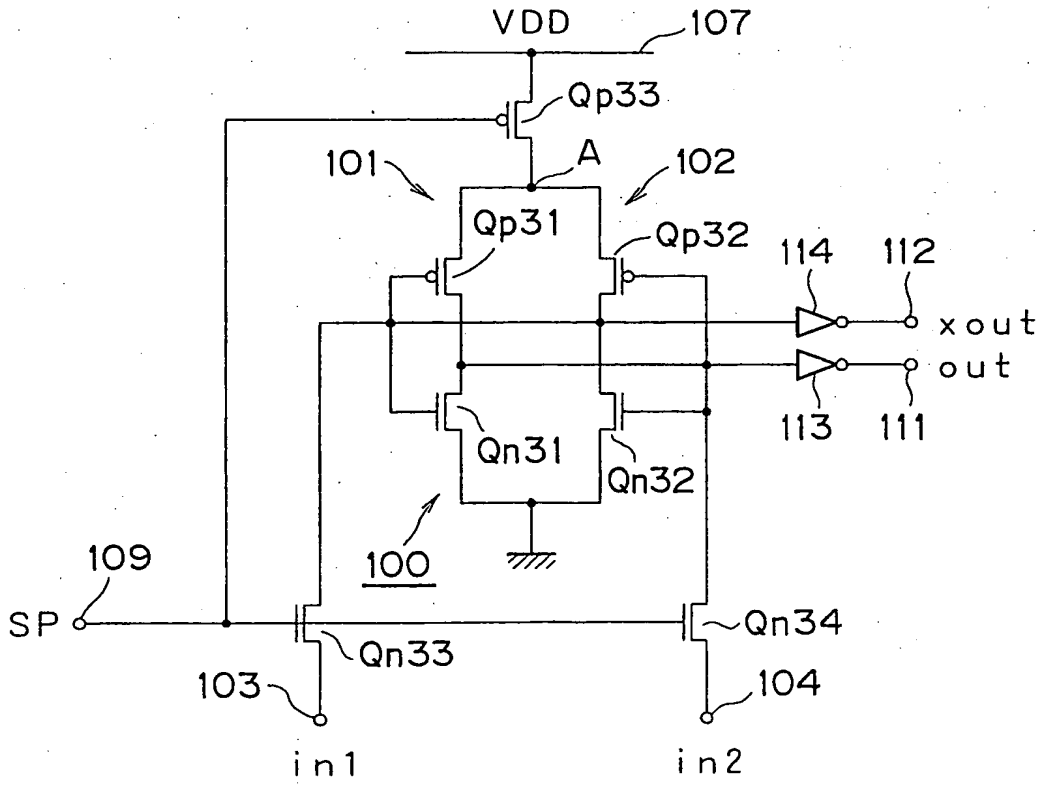

VDD
107
Qp33
101
A
102
Qp31
Qp32
114
112
xout
out
113
111
Qn31
Qn32
100
109
SP
Qn33
Qn34
103
104
in1
in2

FIG. 22

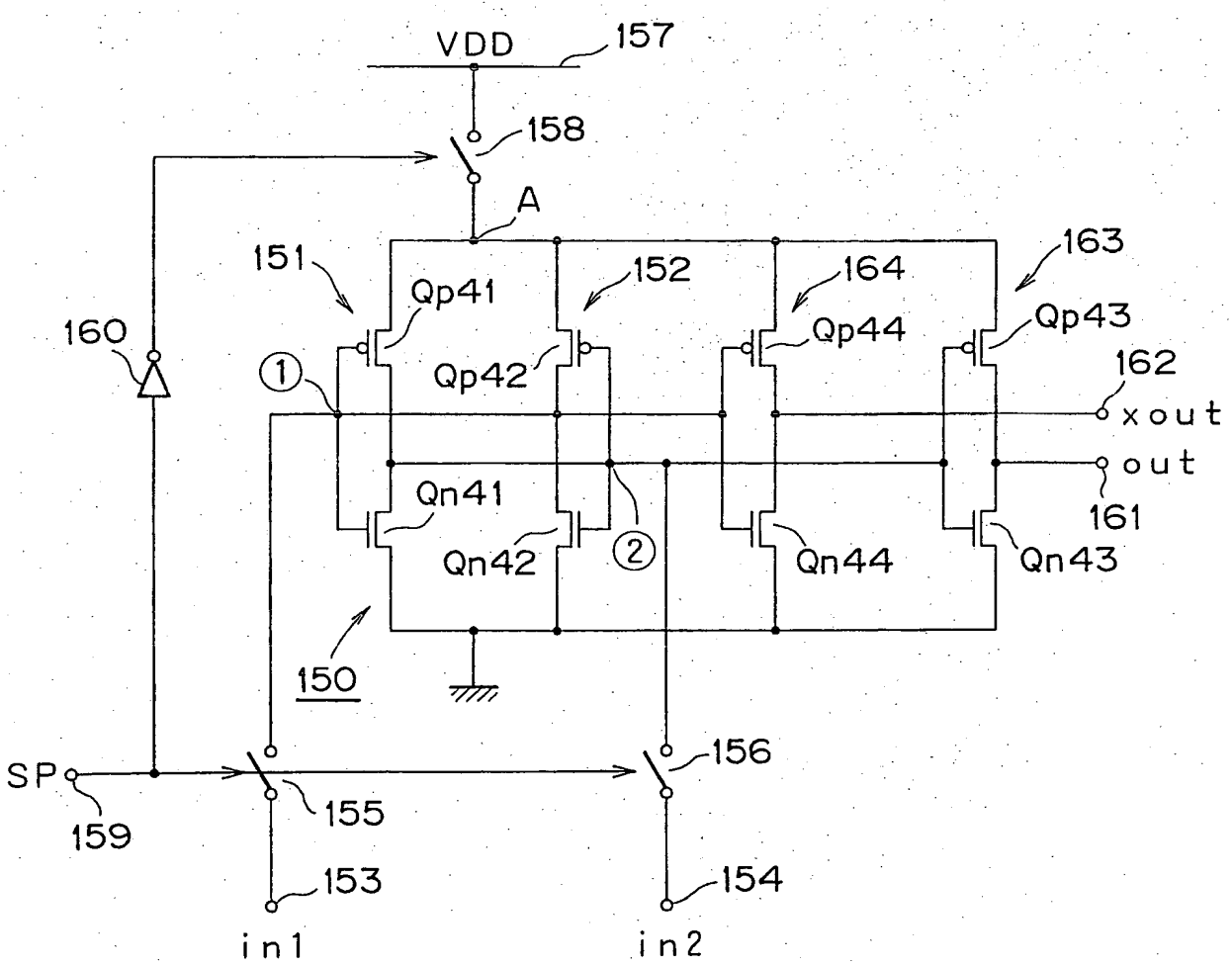

VDD
157
158
A
151
Qp41
152
164
163
Qp44
Qp43
160
Qp42
162
xout
out
Qn41
161
Qn42
Qn44
Qn43
150
SP
156
159
155
153
154
in1
in2

FIG. 23

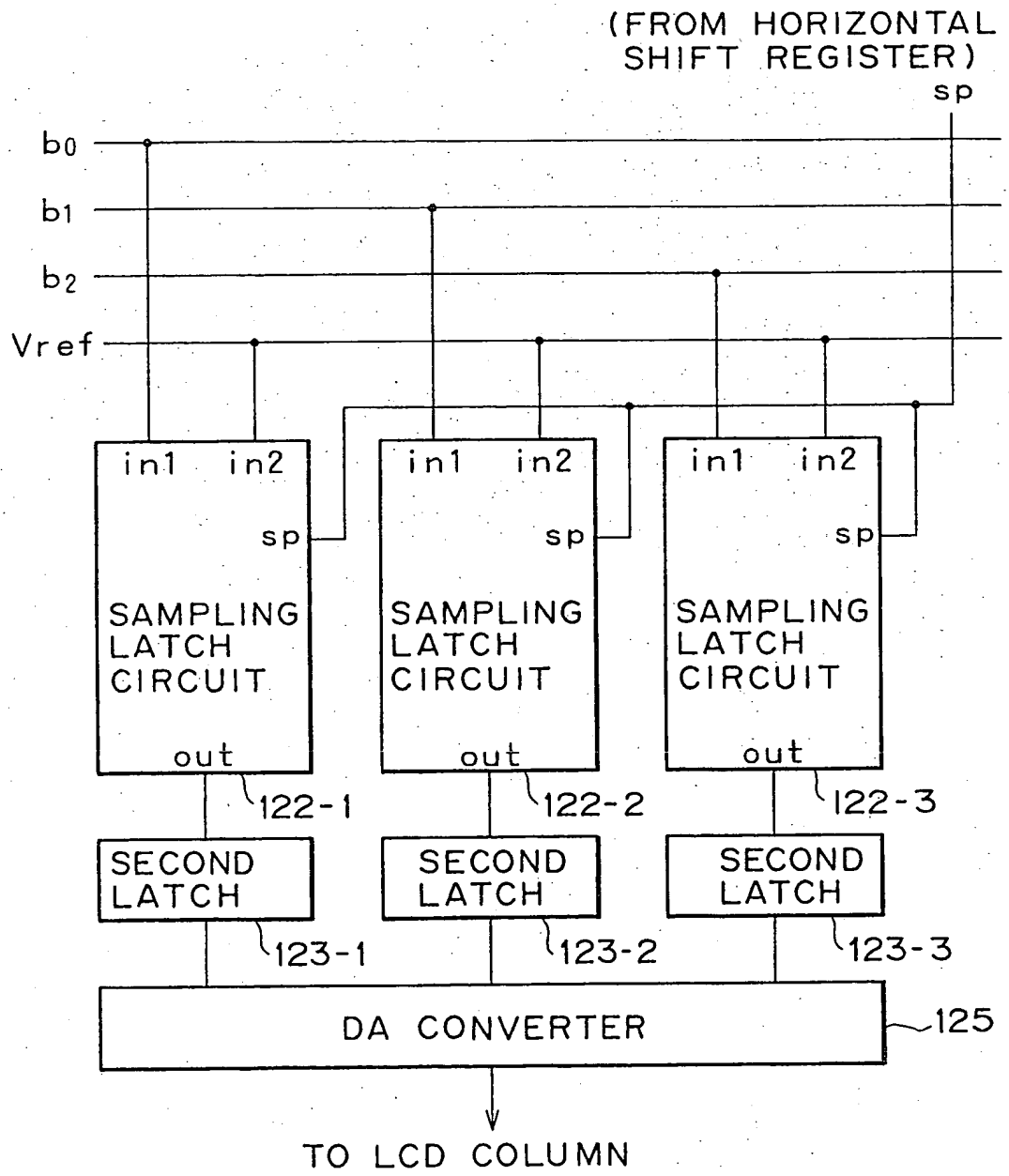

(FROM HORIZONTAL SHIFT REGISTER)
sp
b0
b1
b2
Vref
in1
in2
sp
SAMPLING LATCH CIRCUIT
out
122-1
122-2
122-3
SECOND LATCH
123-1
123-2
123-3
DA CONVERTER
125
TO LCD COLUMN

FIG. 24

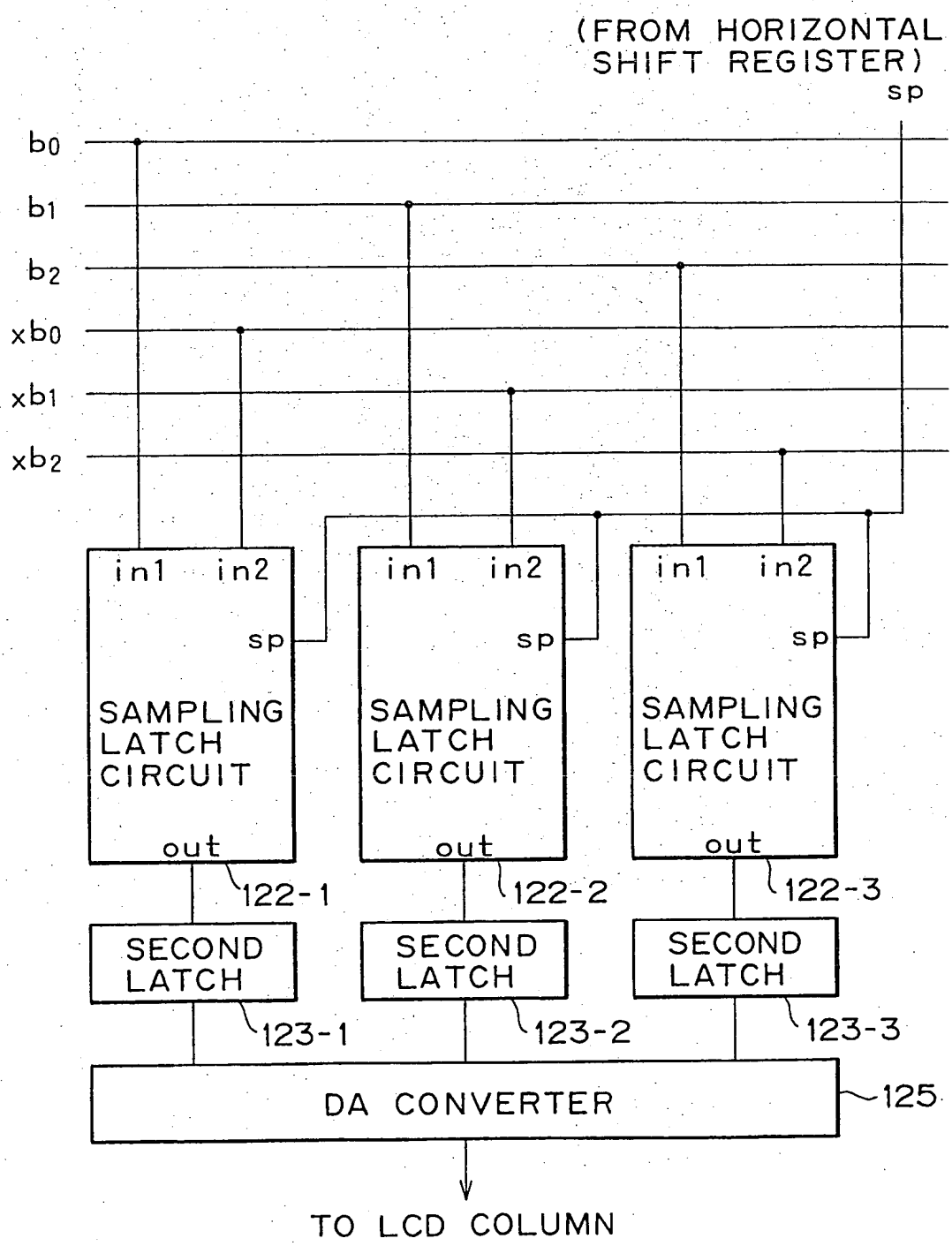

(FROM HORIZONTAL SHIFT REGISTER)
sp
b0
b1
b2
xb0
xb1
xb2
in1
in2
sp
SAMPLING LATCH CIRCUIT
out
122-1
122-2
122-3
SECOND LATCH
123-1
123-2
123-3
DA CONVERTER
125
TO LCD COLUMN

FIG. 25

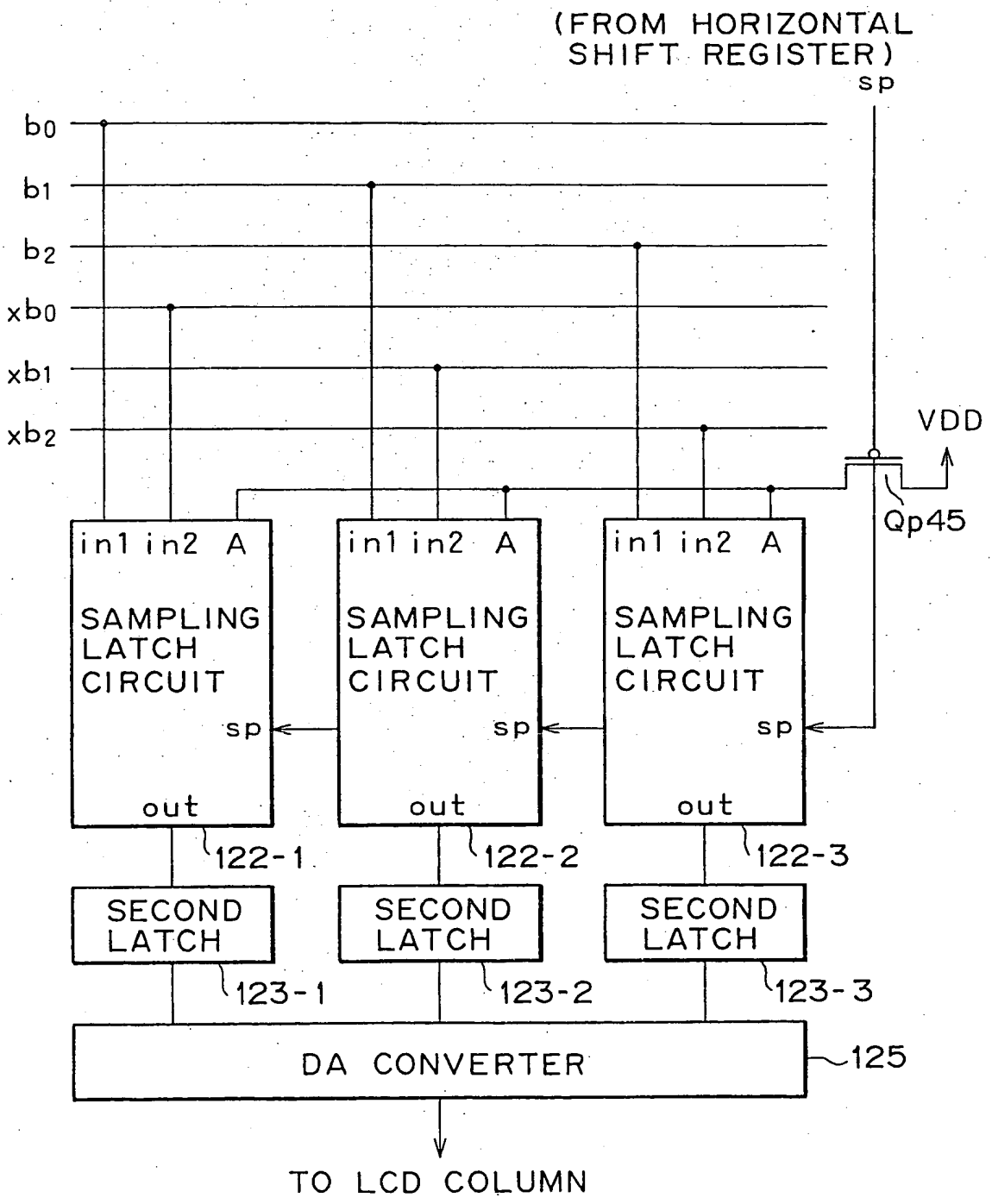

(FROM HORIZONTAL SHIFT REGISTER)
sp
b0
b1
b2
xb0
xb1
xb2
VDD
Qp45
in1 in2 A
SAMPLING LATCH CIRCUIT
sp
out
122-1
122-2
122-3
SECOND LATCH
123-1
123-2
123-3
DA CONVERTER
125
TO LCD COLUMN

FIG. 26

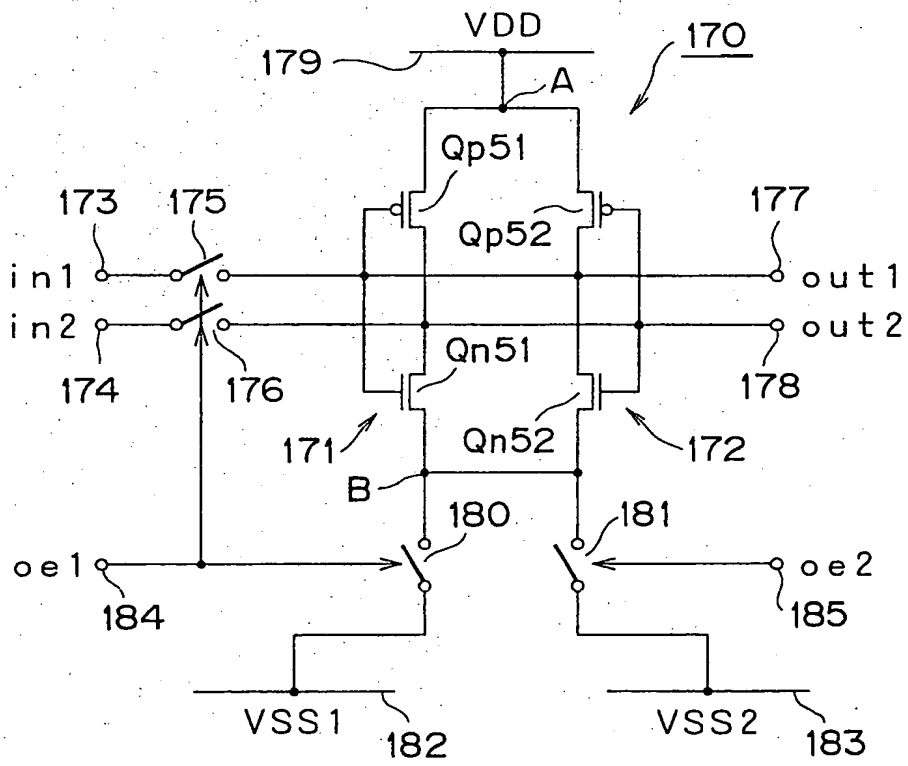

VDD
179
170
A
Qp51
Qp52
173
175
177
in1
out1
in2
out2
Qn51
174
176
178
171
Qn52
172
B
180
181
oe1
oe2
184
185
VSS1
182
VSS2
183

FIG. 27

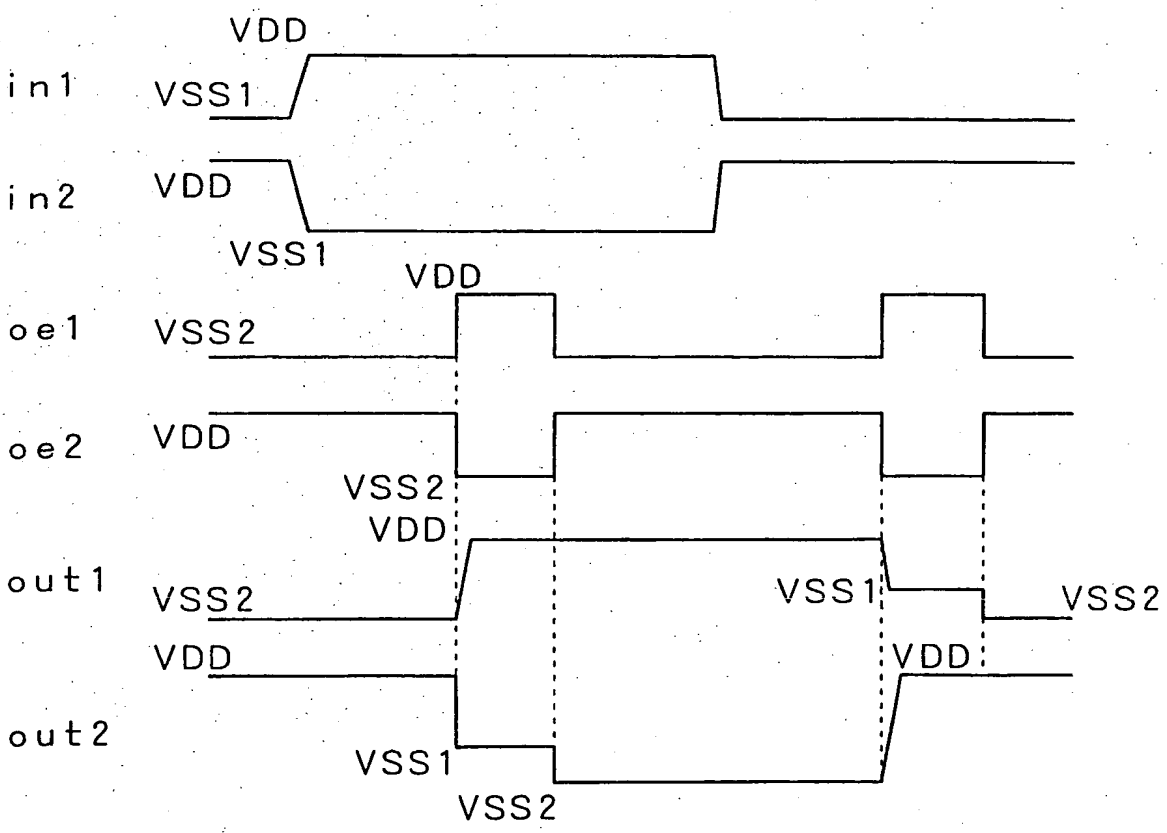

VDD
in1
VSS1
in2
VDD
VSS1
VDD
oe1
VSS2
oe2
VDD
VSS2
VDD
out1
VSS2
VSS1
VSS2
VDD
VDD
out2
VSS1
VSS2

FIG. 28

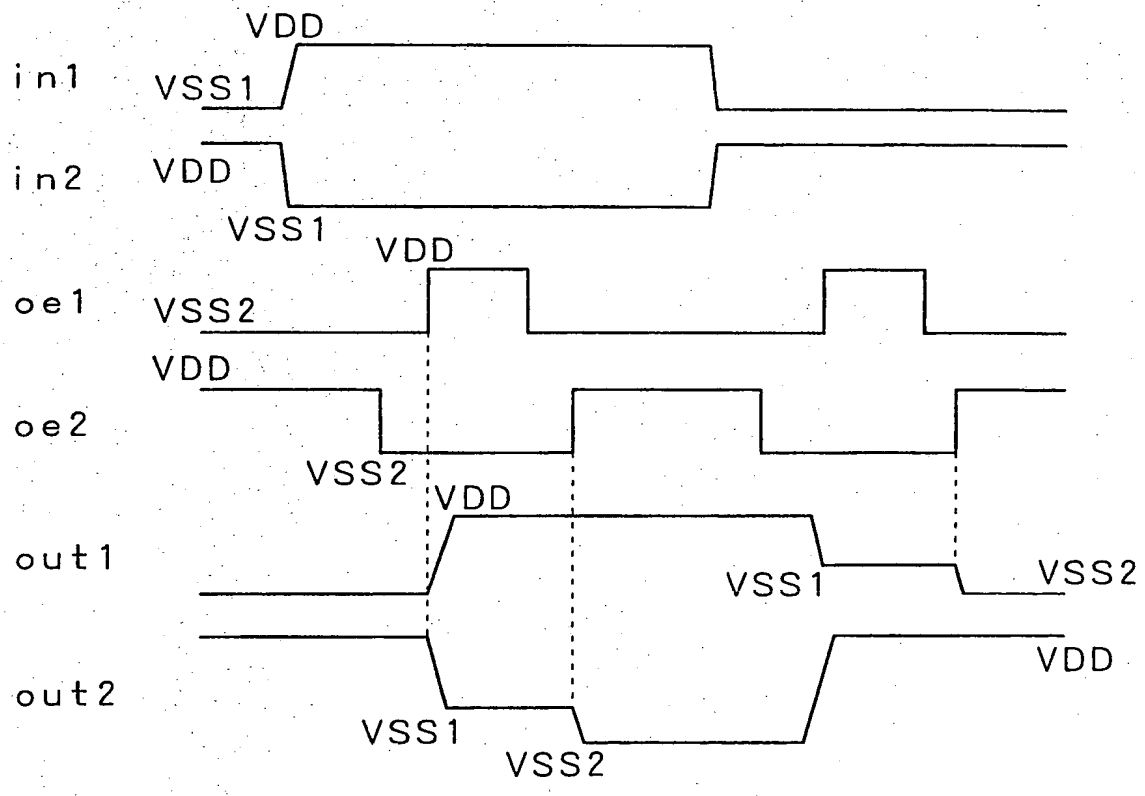

in1
VDD
VSS1
in2
VDD
VSS1
oe1
VDD
VSS2
oe2
VDD
VSS2
out1
VDD
VSS1
VSS2
out2
VDD
VSS1
VSS2

FIG. 29

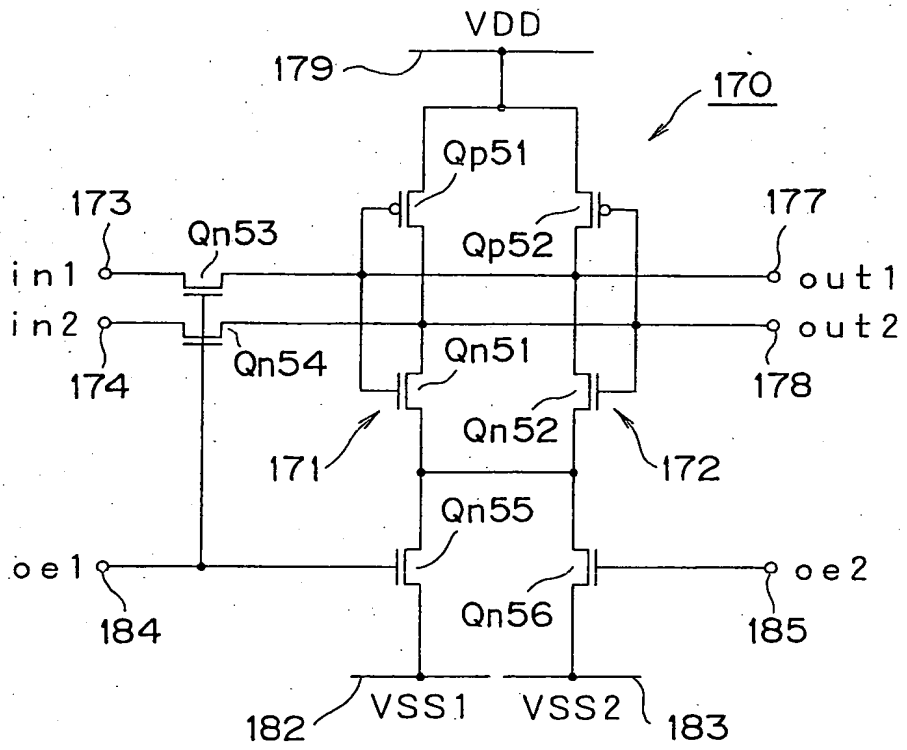

VDD
179
170
Qp51
173
Qn53
Qp52
177
in1
out1
in2
out2
Qn54
Qn51
174
178
Qn52
171
172
Qn55
oe1
oe2
184
Qn56
185
182
VSS1
VSS2
183

FIG. 30

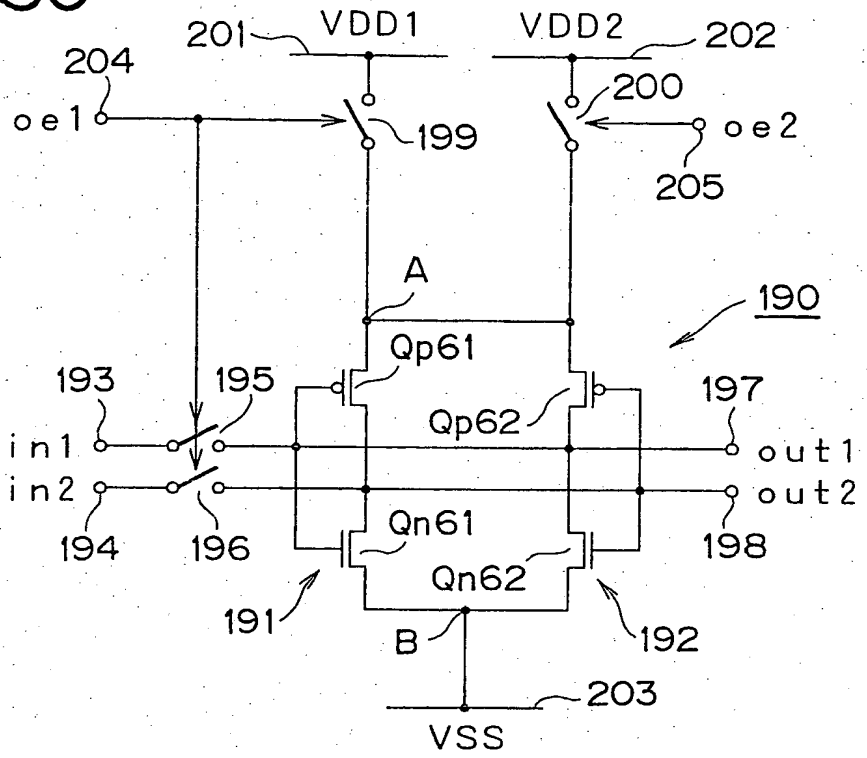

201
VDD1
VDD2
202
204
200
oe1
199
oe2
205
A
190
Qp61
193
195
197
Qp62
in1
out1
in2
out2
Qn61
194
196
198
Qn62
191
192
B
203
VSS

FIG. 31

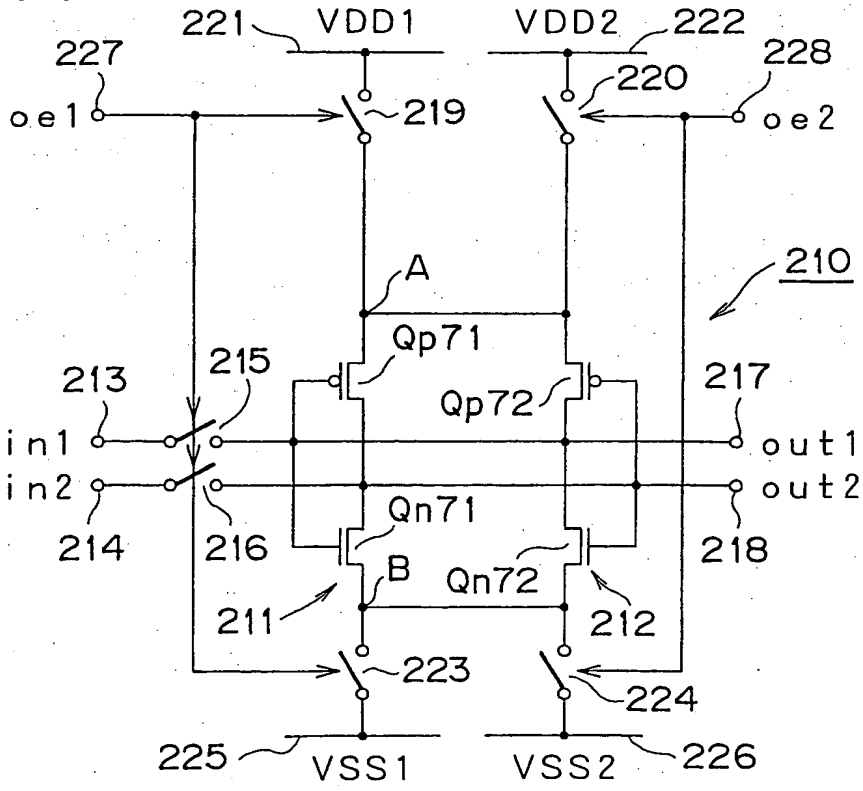

221
VDD1
VDD2
222
227
220
228
oe1
219
oe2
A
210
Qp71
213
215
217
Qp72
in1
out1
in2
out2
Qn71
214
216
218
B
Qn72
211
212
223
224
225
VSS1
VSS2
226

FIG. 32

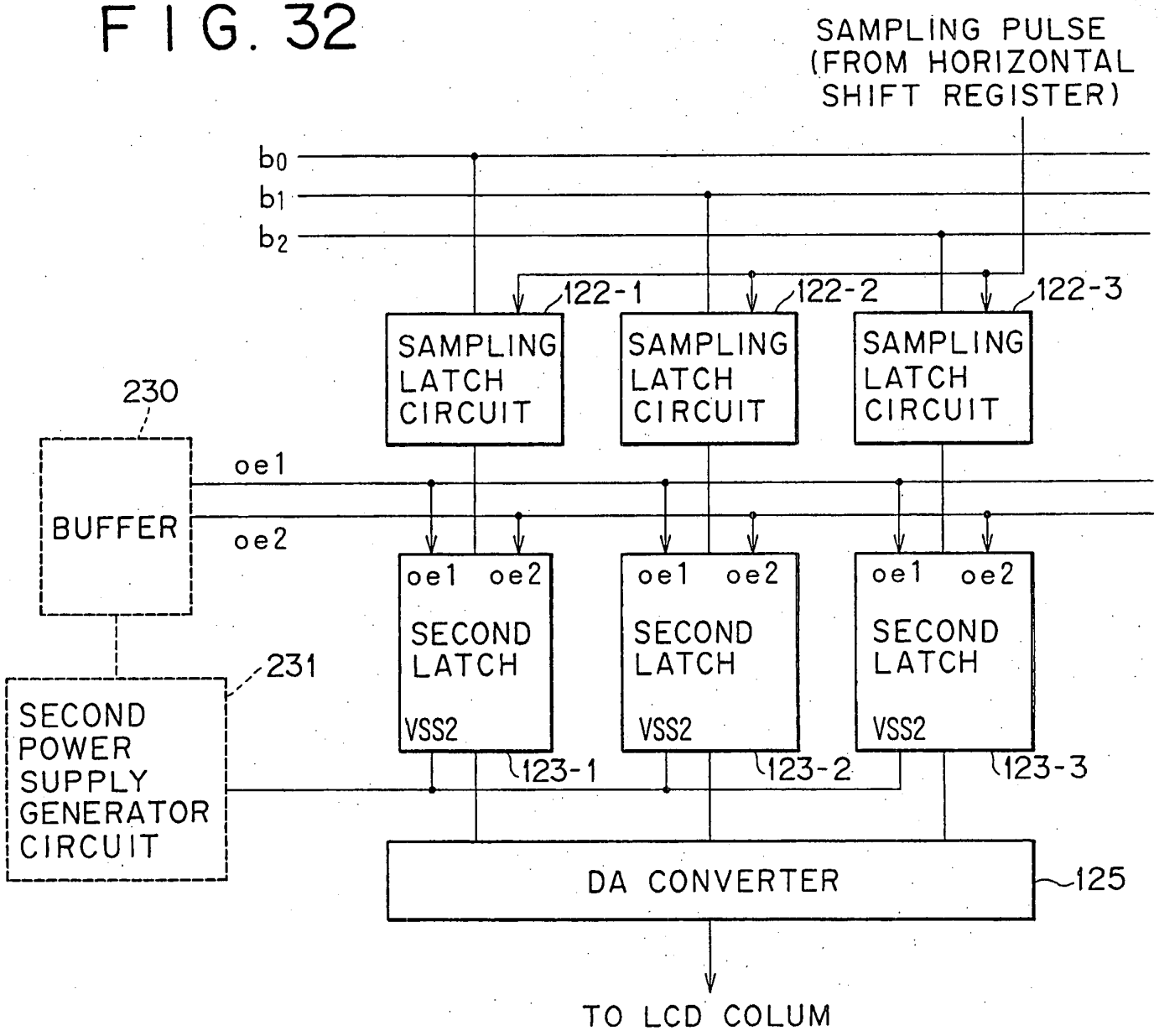

SAMPLING PULSE
(FROM HORIZONTAL
SHIFT REGISTER)
b0
b1
b2
122-1
122-2
122-3
SAMPLING
LATCH
CIRCUIT
SAMPLING
LATCH
CIRCUIT
SAMPLING
LATCH
CIRCUIT
230
BUFFER
oe1
oe2
oe1 oe2
SECOND
LATCH
VSS2
oe1 oe2
SECOND
LATCH
VSS2
oe1 oe2
SECOND
LATCH
VSS2
231
SECOND
POWER
SUPPLY
GENERATOR
CIRCUIT
123-1
123-2
123-3
DA CONVERTER
125
TO LCD COLUM

FIG. 33

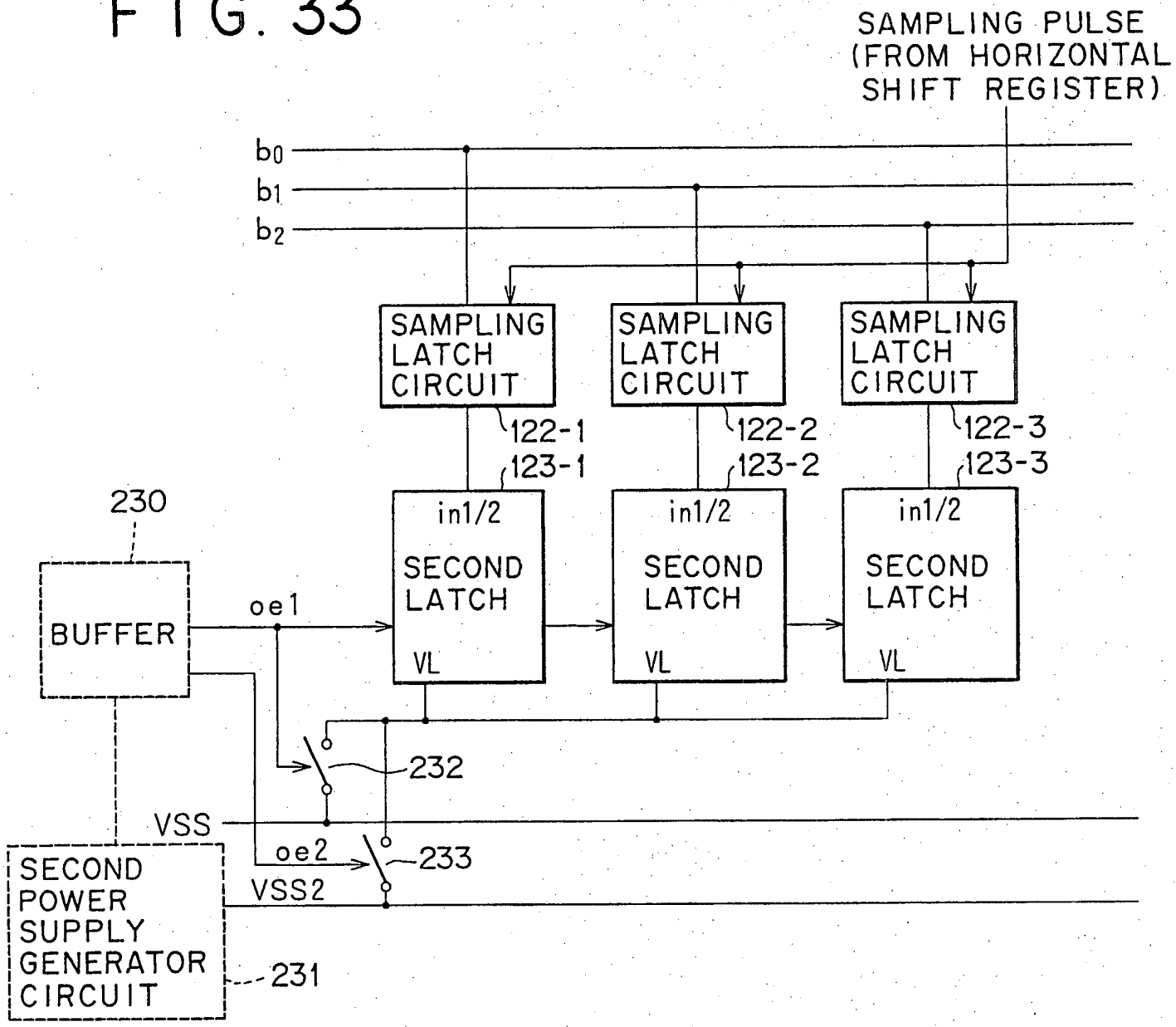

SAMPLING PULSE
(FROM HORIZONTAL
SHIFT REGISTER)
b0
b1
b2
SAMPLING
LATCH
CIRCUIT
SAMPLING
LATCH
CIRCUIT
SAMPLING
LATCH
CIRCUIT
122-1
122-2
122-3
123-1
123-2
123-3
230
in1/2
SECOND
LATCH
VL
in1/2
SECOND
LATCH
VL
in1/2
SECOND
LATCH
VL
BUFFER
oe1
232
VSS
oe2
233
VSS2
SECOND
POWER
SUPPLY
GENERATOR
CIRCUIT
231

FIG. 34

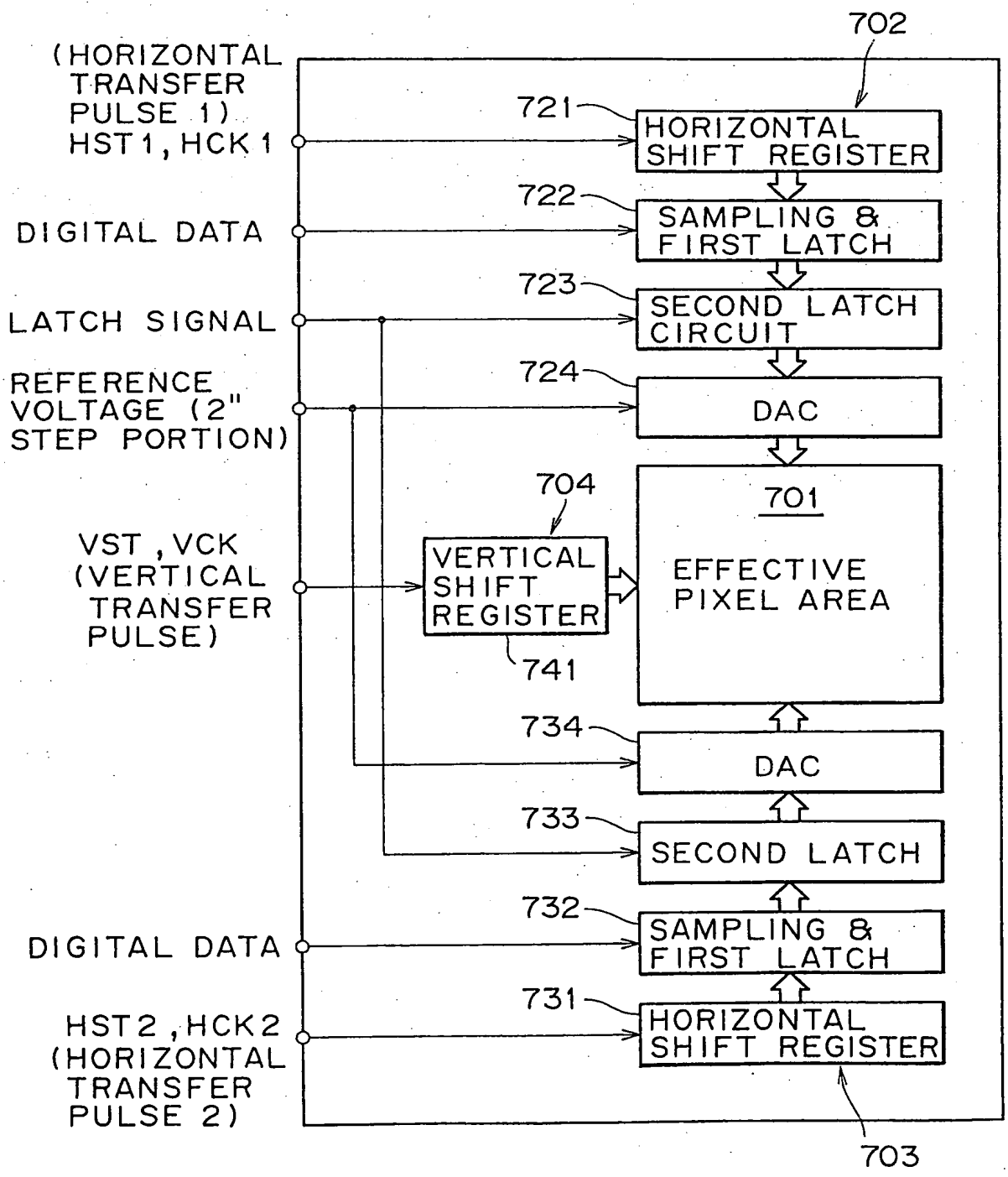
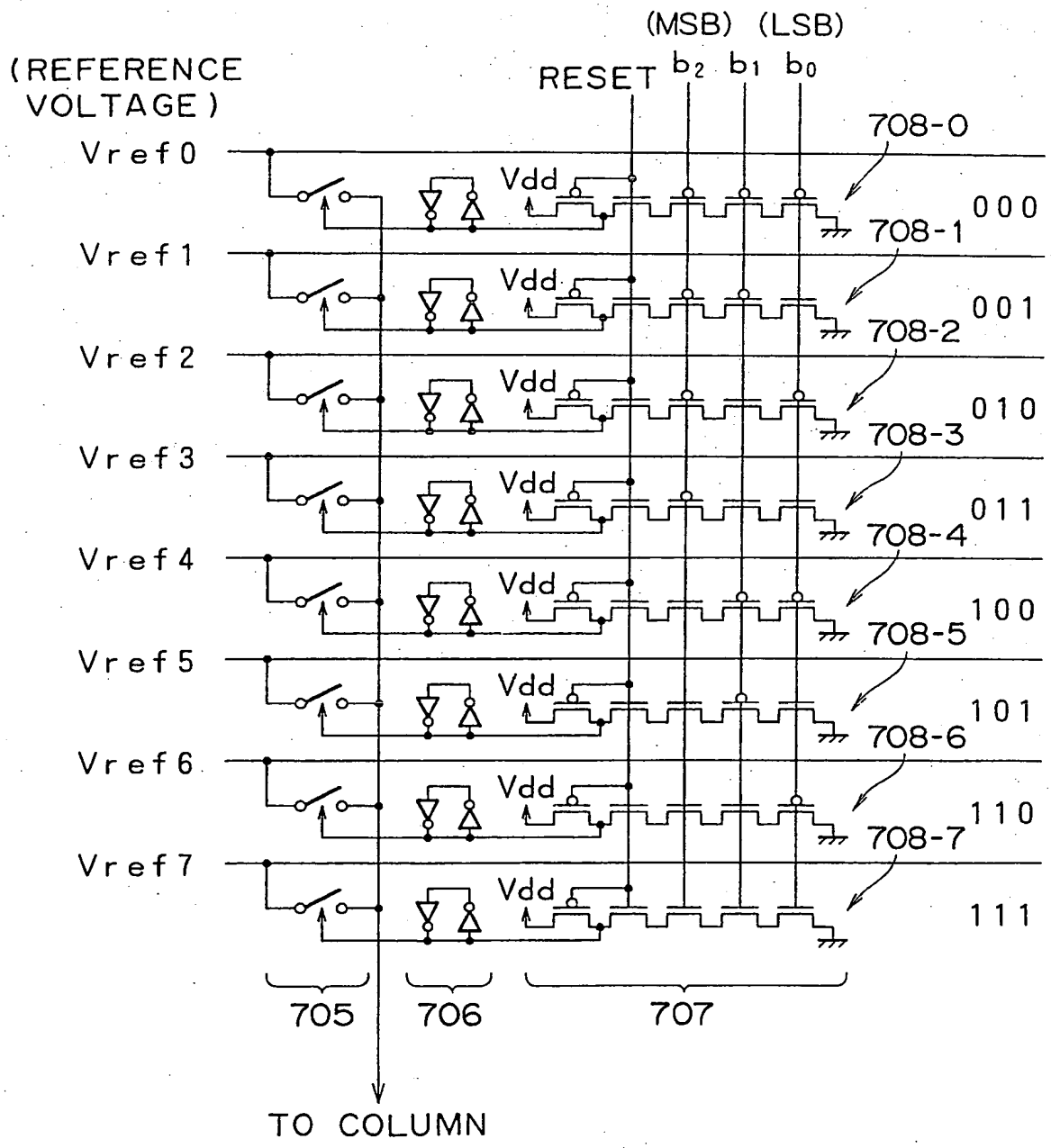

702
(HORIZONTAL TRANSFER PULSE 1) HST1, HCK1
721
HORIZONTAL SHIFT REGISTER
722
DIGITAL DATA
SAMPLING & FIRST LATCH
723
LATCH SIGNAL
SECOND LATCH CIRCUIT
724
REFERENCE VOLTAGE (2" STEP PORTION)
DAC
704
701
VST, VCK (VERTICAL TRANSFER PULSE)
VERTICAL SHIFT REGISTER
EFFECTIVE PIXEL AREA
741
734
DAC
733
SECOND LATCH
732
DIGITAL DATA
SAMPLING & FIRST LATCH
731
HST2, HCK2 (HORIZONTAL TRANSFER PULSE 2)
HORIZONTAL SHIFT REGISTER
703

FIG. 35


(REFERENCE VOLTAGE)
Vref0
Vref1
Vref2
Vref3
Vref4
Vref5
Vref6
Vref7
(MSB) (LSB)
RESET
b2 b1 b0
708-0
708-1
708-2
708-3
708-4
708-5
708-6
708-7
000
001
010
011
100
101
110
111
Vdd
705
706
707
TO COLUMN